

# **JEDEC STANDARD**

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## **DDR5 Registered Dual Inline Memory Module (RDIMM) Common Standard**

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## DDR5 Registered Dual Inline Memory Module (RDIMM) Common Standard

(From JEDEC Board Ballet JCB-26-03, formulated under the cognizance of the JC-45.1 subcommittee on registered DRAM modules, item 2273.07B).

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### 1 Product Description

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This standard defines the electrical and mechanical requirements for 288-position, 1.1 Volt (VDD and VDDQ), DDR5 Registered (RDIMM), Double Data Rate (DDR), Synchronous DRAM Dual In-Line Memory Modules (DIMM). These Registered DDR5 SDRAM DIMMs are intended for use in server, workstation, and database environments.

Reference design examples are included which provide an initial basis for DDR5 RDIMM design. Modifications to these reference designs may be required to meet all system timing, signal integrity and thermal requirements for PC5-4000 through PC5-9200 data rate support. All DDR5 RDIMM implementation must use simulations and lab verification to ensure proper timing requirements, signal integrity, power delivery, and efficiencies in the design.

#### 1.1 Normative References

JESD79-5, *DDR5 SDRAM*

JESD300-5, *SPD5118 Hub and Serial Presence Detect Device Standard*

JESD301-1, *PMIC5000/PMIC5010 Power Management IC Standard*

JESD301-4, *PMIC5020 Power Management IC Standard*

JESD301-5, *PMIC5030 Power Management IC Standard*

JESD302-1, *TS5111, TS5110 Serial Bus Thermal Sensor Device Standard*

JESD400-5, *DDR5 Serial Presence Detect (SPD) Contents*

JESD401-5, *DDR5 DIMM Label*

JESD402-1, *Temperature Range and Measurement Standard for Components and Modules*

JESD403-1, *JEDEC Module Sideband Bus (SidebandBus)*

JESD82-51[4:1]x, *DDR5RCD0x Full Standard (04 through 01)*

MO-210, *Square and Rectangular Die-Size, Ball Grid Array Family*

MO-329, *288 PIN DDR5 DIMM, 0.85 mm pitch*

## 1.1 Normative References (cont'd)

**Table 1 — DDR5 Product Family Attributes**

DIMM Organization	x80 (2x40) ECC (EC8) x72 (2x36) ECC (EC4)	Notes	Reference Standards
<b>DIMM Dimensions (nom)</b>	133.35 mm x 31.25 mm		MO-329
<b>Position Count</b>	288		MO-329
<b>DDR5 SDRAMs Supported</b>	8Gb, 16Gb, 24Gb, 32Gb	78/82-ball FBGA package for x4 and x8 devices	JESD79-5 MO-210 (AL, AN)
<b>Capacity</b>	8Gb – 8GB – 512GB 16Gb - 16GB - 1024GB 24Gb - 24GB – 1536GB 32Gb - 32GB – 2048GB	(SDRAM) SDP, 3DS (2H, 4H, 8H, 16H)	
<b>SDRAM width</b>	x4, x8		
<b>Hub with Thermal Sensor</b>	1024 byte		JESD301-1 JESD301-4 JESD301-5 JESD300-5 JESD79-5
<b>Voltage (External Supply)</b>	VIN_BULK: 12V (nominal)	Bulk input DC supply voltage from system	
	VIN_MGMT: 3.3V (nominal)	Management supply voltage from system	
<b>Voltage (PMIC Output)</b>	VDD: 1.1 V (nominal)	Supply voltage from PMIC	
	VDDQ: 1.1 V (nominal)	Supply voltage for I/O from PMIC	
	VPP: 1.8 V (nominal)	Pump voltage from PMIC	
	1.8V LDO (nominal)	From PMIC to HUB, TS	
	1.0V LDO Output (nominal)	From PMIC to HUB, TS, RCD	
<b>DDR5 Interface</b>	1.1V signaling	SDRAM, RCD	
<b>I2C/I3C-Basic Interface</b>	1.0V to 3.3V signaling (mode dependent)	RCD, Hub, PMIC, Temp Sensors	JESD403-1 JESD300-5

## 2 Environmental Requirements

**Table 2 — (Example) Environmental Parameters**

Symbol	Parameter	Rating	Units
<b>TOPR</b>	SDRAM Operating Temperature	0 to +95	°C
<b>TSTG</b>	Storage Temperature	-55 to +100	°C
<p>NOTE 1 Operating temperature applies to the case temperature of all SDRAM components on the module. All other support components on the module must remain within their respective operating temperature ranges when the case temperature of the SDRAMs is at the minimum and maximum values. See JESD402-1 for details.</p> <p>NOTE 2 Storage temperature applies to the case temperature of all components on the module. See JESD402-1 for details. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.</p>			

## 3 Connector Pinout and Signal Description

**Table 3 — Pin Definitions**

Pin Name	Description	Pin Name	Description
<b>CA[6:0]_A</b> <b>CA[6:0]_B</b>	Command and Address (CA) Bus	<b>DQ[31:0]_A</b> <b>DQ[31:0]_B</b>	DIMM memory Data bus channel A and B
<b>CS[1:0]_A_n</b> <b>CS[1:0]_B_n</b>	Control (Chip Select) (CS_n)	<b>CB[7:0]_A</b> <b>CB[7:0]_B</b>	DIMM ECC Checkbits (CB) channel A and B
<b>PAR_A</b> <b>PAR_B</b>	Parity input	<b>DQS[9:0]_A_t</b> <b>DQS[9:0]_B_t</b>	Data Strobes (positive line of differential pair)
<b>CK_t</b>	Clock (true/positive)	<b>DQS[9:0]_A_c</b> <b>DQS[9:0]_B_c</b>	Data Strobes (negative line of differential pair)
<b>CK_c</b>	Clock (complement/negative)	<b>TDQS[9:5]_A_t</b> <b>TDQS[9:5]_B_t</b>	Not valid for x4 operation. Enabled via Mode Register.
<b>ALERT_n</b>	Alert for CRC error	<b>TDQS[9:5]_A_c</b> <b>TDQS[9:5]_B_c</b>	Not valid for x4 operation. Enabled via Mode Register.
<b>RESET_n</b>	Set SDRAM to known state	<b>VIN_BULK</b>	DIMM Power Supply from system to PMIC
<b>PCAMP</b>	Control and Monitor Port	<b>VIN_MGMT</b>	DIMM Power Supply from system to PMIC
<b>HSCL</b>	I2C/I3C-Basic Host Sideband Bus Clock	<b>VSS</b>	Power supply return (ground)
<b>HSDA</b>	I2C/I3C-Basic Host Sideband Bus Data	<b>RFU</b>	Reserved for future use
<b>HSA</b>	I2C/I3C-Basic Host Sideband Bus Address		
<b>LBDQ</b>	Loopback Data output:		
<b>LBDQS</b>	Loopback Data strobe output		
NOTE 1 TDQSx and DQSx_t share a pin.			

### 3 Connector Pinout and Signal Description (cont'd)

**Table 4 — Input/Output Functional Description**

Symbol	Type	I/O Levels	Function
<b>CK_t, CK_c,</b>	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All CA and CS_n input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
<b>CA[6:0]_A CA[6:0]_B</b>	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi-cycle, the pins may not be interchanged between devices on the same bus. The address inputs also provide the op-code during Mode Register Set commands.
<b>CS[1:0]_A_n CS[1:0]_B_n</b>	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command codes. CS_n is also used to enter and exit the parts from power down mode and self-refresh mode. While not in self-refresh mode the CS_n input buffer operates with the same ODT and VREF parameters as configured by the CA_ODT strap setting or mode register. When in self-refresh the CS_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD.
<b>PAR_A PAR_B</b>	Input	VDD	Each CA input parity is received on the DPAR pin and should maintain even parity across the channel CA inputs. DPAR is sampled at the rising and falling edges of the input clock.
<b>ALERT_n</b>	Output	VDD	Alert: If there is an error in CRC, then ALERT_n shall drive LOW for the period time interval and return HIGH. During Connectivity Test mode, this pin functions as an input. Usage of this signal or not is system dependent. In case this pin is not connected, ALERT_n pin must be bonded to VDDQ on the system board.
<b>RESET_n</b>	CMOS Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.  RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ.
<b>PCAMP</b>	Input Output	3.6V (max)	Control and Monitor Port. Provides three different functions: (1) Register write protect function; (2) Fail_n function; and (3) Status function (PWR_GOOD).
<b>HSCL</b>	Input	1.0V – 3.3V	Bus clock used to strobe data into HUB device. When open drain, a pullup resistor is required on the system motherboard. Refer to JESD300-5 and JESD403-1.
<b>HSDA</b>	Input/ Output	1.0V – 3.3V	I2C/I3C-Basic data. When Open drain, a pullup resistor is required on the system motherboard. Refer to JESD300-5 and JESD403-1.
<b>HSA</b>	Input	2.1V max	Device address for the HUB. Tied to GND through resistor for HID in normal operation and directly to GND in tester operation
<b>DQ[31:0]_A DQ[31:0]_B</b>	Input/ Output	VDD	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register, then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used.
<b>CB[7:0]_A CB[7:0]_B</b>	Input/ Output	VDD	ECC Checkbits Input/ Output: Bi-directional data bus - for 8-bit ECC (EC8) all 8 bits are used - for 4-bit ECC (EC4) [3:0] bits are used; [7:4] bits are floating

**Table 4 — Input/Output Functional Description (cont'd)**

Symbol	Type	I/O Levels	Function
<b>DQS[9:0]_A_t</b> <b>DQS[9:0]_B_t</b>	Input/ Output	VDD	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The Data Strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR5 SDRAM supports differential Data Strobe only and does not support single-ended.
<b>DQS[9:0]_A_c</b> <b>DQS[9:0]_B_c</b>			
<b>TDQS[9:5]_A_t</b> <b>TDQS[9:5]_B_t</b>	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.
<b>TDQS[9:5]_A_c</b> <b>TDQS[9:5]_B_c</b>	Input	VDD	Dummy load for matching the loading for mixed populations of x8 based RDIMMs and x4 based RDIMMs.
<b>DLBDQ</b>	Output	VDDQ	Loopback Data output: The output of this device on the Loopback Output Select defined in MR53:OP[4:0]. When Loopback is enabled, it is in driver mode using the default RON described in the Loopback Function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36: OP[2:0].
<b>DLBDQS</b>	Output	VDDQ	Loopback Data Strobe output: This is a single ended strobe with the rising edged aligned with Loopback Data edge, falling edge aligned with Data center. When Loopback is enabled it is in driver mode using the default RON described in the Loopback function section. When Loopback is disabled, the pin is either terminated or Hi-Z based on MR36: OP[2:0].
<b>RFU</b>			Reserved for Future Use: No on DIMM electrical connection is present.
<b>VIN_BULK</b>	Supply		External power supply: 12 V, 4.25 V (min), 15 V (max)
<b>VIN_MGMT</b>	Supply		External power supply: 3.3 V, 3.0 V (min), 3.6 V (max)
<b>VSS</b>	Supply		Ground

### 3 Connector Pinout and Signal Description (cont'd)

**Table 5 — DDR5 288 Position RDIMM Pin Wiring Assignments**

Front Side Pin Label	Pin	Pin	Back side Pin Label	Front Side Pin Label	Pin	Pin	Back side Pin Label
VIN_BULK	1	145	VIN_BULK	PAR_A	74	218	CK_c
RFU	2	146	VIN_BULK	VSS	75	219	VSS
VIN_MGMT	3	147	PCAMP		Key		
HSCL	4	148	HSA				
HSDA	5	149	RFU	CA0_B	76	220	RFU / No Pin Present
VSS	6	150	RFU	VSS	77	221	CA1_B
DQ0_A	7	151	VSS	CA2_B	78	222	VSS
VSS	8	152	DQ2_A	VSS	79	223	CA3_B
DQ1_A	9	153	VSS	CA4_B	80	224	VSS
VSS	10	154	DQ3_A	VSS	81	225	CA5_B
DQS0_A_t	11	155	VSS	CA6_B	82	226	VSS
DQS0_A_c	12	156	DQS5_A_c, TDQS5_A_c	VSS	83	227	PAR_B
VSS	13	157	DQS5_A_t, TDQS5_A_t	CS0_B_n	84	228	VSS
DQ4_A	14	158	VSS	VSS	85	229	CS1_B_n
VSS	15	159	DQ6_A	DLBDQ	86	230	VSS
DQ5_A	16	160	VSS	DLBDQS	87	231	RFU
VSS	17	161	DQ7_A	VSS	88	232	RFU
DQ8_A	18	162	VSS	CB4_B	89	233	VSS
VSS	19	163	DQ10_A	VSS	90	234	CB6_B
DQ9_A	20	164	VSS	CB5_B	91	235	VSS
VSS	21	165	DQ11_A	VSS	92	236	CB7_B
DQS1_A_t	22	166	VSS	DQS9_B_t, TDQS9_B_t	93	237	VSS
DQS1_A_c	23	167	DQS6_A_c, TDQS6_A_c	DQS9_B_c, TDQS9_B_c	94	238	DQS4_B_c
VSS	24	168	DQS6_A_t, TDQS6_A_t	VSS	95	239	DQS4_B_t
DQ12_A	25	169	VSS	CB0_B	96	240	VSS
VSS	26	170	DQ14_A	VSS	97	241	CB2_B
DQ13_A	27	171	VSS	CB1_B	98	242	VSS
VSS	28	172	DQ15_A	VSS	99	243	CB3_B
DQ16_A	29	173	VSS	DQ0_B	100	244	VSS
VSS	30	174	DQ18_A	VSS	101	245	DQ2_B
DQ17_A	31	175	VSS	DQ1_B	102	246	VSS
VSS	32	176	DQ19_A	VSS	103	247	DQ3_B
DQS2_A_t	33	177	VSS	DQS0_B_t	104	248	VSS
DQS2_A_c	34	178	DQS7_A_c, TDQS7_A_c	DQS0_B_c	105	249	DQS5_B_c, TDQS5_B_c
VSS	35	179	DQS7_A_t, TDQS7_A_t	VSS	106	250	DQS5_B_t, TDQS5_B_t
DQ20_A	36	180	VSS	DQ4_B	107	251	VSS
VSS	37	181	DQ22_A	VSS	108	252	DQ6_B
DQ21_A	38	182	VSS	DQ5_B	109	253	VSS

**Table 5 — DDR5 288 Position RDIMM Pin Wiring Assignments (cont'd)**

Front Side	Pin	Pin	Back side	Front Side	Pin	Pin	Back side
Pin Label			Pin Label	Pin Label			Pin Label
VSS	39	183	DQ23_A	VSS	110	254	DQ7_B
DQ24_A	40	184	VSS	DQ8_B	111	255	VSS
VSS	41	185	DQ26_A	VSS	112	256	DQ10_B
DQ25_A	42	186	VSS	DQ9_B	113	257	VSS
VSS	43	187	DQ27_A	VSS	114	258	DQ11_B
DQS3_A_t	44	188	VSS	DQS1_B_t	115	259	VSS
DQS3_A_c	45	189	DQS8_A_c, TDQS8_A_c	DQS1_B_c	116	260	DQS6_B_c, TDQS6_B_c
VSS	46	190	DQS8_A_t, TDQS8_A_t	VSS	117	261	DQS6_B_t, TDQS6_B_t
DQ28_A	47	191	VSS	DQ12_B	118	262	VSS
VSS	48	192	DQ30_A	VSS	119	263	DQ14_B
DQ29_A	49	193	VSS	DQ13_B	120	264	VSS
VSS	50	194	DQ31_A	VSS	121	265	DQ15_B
CB0_A	51	195	VSS	DQ16_B	122	266	VSS
VSS	52	196	CB2_A	VSS	123	267	DQ18_B
CB1_A	53	197	VSS	DQ17_B	124	268	VSS
VSS	54	198	CB3_A	VSS	125	269	DQ19_B
DQS4_A_t	55	199	VSS	DQS2_B_t	126	270	VSS
DQS4_A_c	56	200	DQS9_A_c, TDQS9_A_c	DQS2_B_c	127	271	DQS7_B_c, TDQS7_B_c
VSS	57	201	DQS9_A_t, TDQS9_A_t	VSS	128	272	DQS7_B_t, TDQS7_B_t
CB4_A	58	202	VSS	DQ20_B	129	273	VSS
VSS	59	203	CB6_A	VSS	130	274	DQ22_B
CB5_A	60	204	VSS	DQ21_B	131	275	VSS
VSS	61	205	CB7_A	VSS	132	276	DQ23_B
ALERT_n	62	206	VSS	DQ24_B	133	277	VSS
VSS	63	207	RESET_n	VSS	134	278	DQ26_B
CS0_A_n	64	208	VSS	DQ25_B	135	279	VSS
VSS	65	209	CS1_A_n	VSS	136	280	DQ27_B
CA0_A	66	210	VSS	DQS3_B_t	137	281	VSS
VSS	67	211	CA1_A	DQS3_B_c	138	282	DQS8_B_c, TDQS8_B_c
CA2_A	68	212	VSS	VSS	139	283	DQS8_B_t, TDQS8_B_t
VSS	69	213	CA3_A	DQ28_B	140	284	VSS
CA4_A	70	214	VSS	VSS	141	285	DQ30_B
VSS	71	215	CA5_A	DQ29_B	142	286	VSS
CA6_A	72	216	VSS	VSS	143	287	DQ31_B
VSS	73	217	CK_t	RFU	144	288	VSS

NOTE 1 Individual Annex standards for RDIMM define pin use where multiple functions are possible.

NOTE 2 Pin 220 for 8000 Mbps and faster RDIMM raw cards do not have the edge pin present.

## 4 Power Details

### 4.1 DIMM Voltage Requirements and Power-Up Sequence

The DIMM input voltage requirements and the SDRAM voltage requirements are not identical. The DIMM voltage requirements must meet the PMIC input voltage requirements. The PMIC output voltage requirements must meet the voltage requirements of SDRAM, RCD, Hub and Temperature Sensors. There must be some allowance for a small voltage drop across the DIMM for both supply voltages and PMIC output voltages. Table 6 defines the requirements from the Host at the DIMM socket to the PMIC inputs, and the PMIC outputs.

Some DIMMs have lower current requirements. Each specific DIMM configuration must meet the voltage requirements for its worst-case load currents.

**Table 6 — DDR5 RDIMM DC Operating Voltage**

Symbol	Parameter	Voltage Rating (Volts)			Expected Current (Amps) <sup>3</sup>	Power State
		Minimum	Typical <sup>4</sup> (Nominal)	Maximum		
<b>VIN_BULK</b>	Host Supply Voltage	4.25	12.0	15	2.5 (maximum)	Operational
<b>VIN_MGMT</b>	Host Supply Voltage	3.0	3.3	3.6	0.110 (maximum)	Operational
<b>VDD<sup>1</sup></b>	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
<b>VDDQ<sup>1</sup></b>	PMIC Output Supply Voltage	1.067	1.1	1.166	Note 5	Operational
<b>VPP<sup>1</sup></b>	PMIC Output Supply Voltage	1.746	1.8	1.908	Note 5	Operational
<b>1.8V LDO<sup>2</sup></b>	PMIC Output Supply Voltage	Note 6	1.8	Note 6	0.025 (maximum)	Operational
<b>1.0V LDO<sup>2</sup></b>	PMIC Output Supply Voltage	Note 6	1.0	Note 6	0.020 (maximum)	Operational
NOTE 1 The DDR5 SDRAM Standard must be met and takes precedence over this document. NOTE 2 PMIC, Hub, TS, RCD Standards must be met and take precedence over this document. NOTE 3 Maximum current establishes the platform maximum current regulation point. It provides a data point for DIMM developers to set power plane impedances. NOTE 4 Typical voltage is platform dependent. This is a suggested value only. NOTE 5 Maximum and Minimum Current ratings depend on PMIC 5000, 5010, 5020, 5030 and number of SDRAM die placed. NOTE 6 See PMIC supplier datasheets for Minimum and Maximum ratings.						

### 4.2 Rules for PMIC Power-Up Sequence

Refer to JESD301-1 PMIC5000, PMIC5010, JESD301-4 PMIC5020, and JESD301-5 PMIC5030 Power Management IC Standards for sequence requirements.

### 4.3 Rules for PMIC Power Down Sequence

Refer to JESD301-1 PMIC5000, PMIC5010, JESD301-4 PMIC5020, and JESD301-5 PMIC5030 Power Management IC Standards for sequence requirements.

### 4.4 Rules for VDD and VDDQ Power Planes

VDD and VDDQ are nominally the same voltage. Reference designs for RDIMM raw cards will have individual planes for each voltage rail.



5 Component Details

The active components on the DIMM are the DDR5 SDRAM, RCD, PMIC, Temperature Sensor, and Hub.

- The DDR5 SDRAM x4 and x8 are defined in JESD79-5 and MO-210
- The RCD component is defined in JESD82-511/512/513/514 with MO-330, and JESD82-515 with MO-361.
- The PMIC is defined in JESD301-1, JESD301-4, JESD301-5, and MO-333
- The Temperature Sensor is defined in JESD302-1
- The Hub (SPD) is defined in JESD300-5 and MO-229

The Annex Standards for each reference design will identify the maximum SDRAM package size the layout will accept. The SDRAM terminal pattern will determine if support balls are present in the reference design. Reference JEDEC MO-210 for DDR5 SDRAM terminal pattern features.

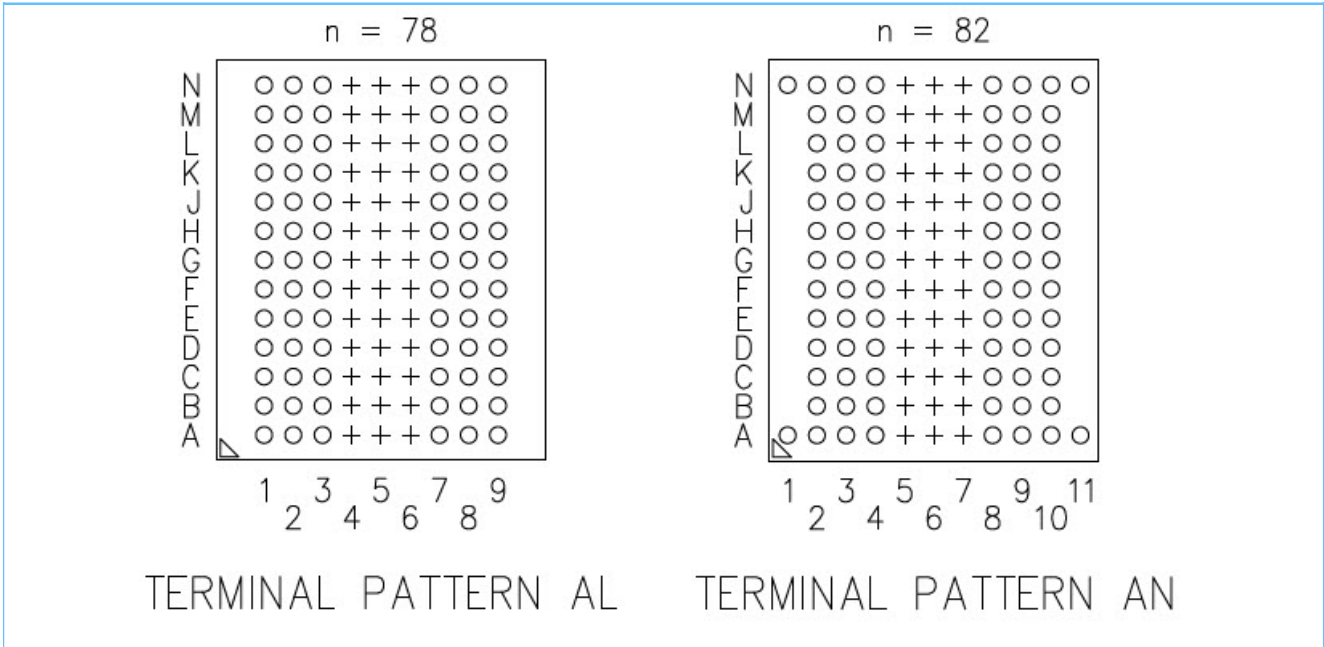


Figure 1 — DDR5 SDRAM Terminal Patterns (x4/x8)

## 5 Component Details (cont'd)

**Table 7 — DDR5 x4/X8 SDRAM DIMM Pad Array**

Top View - (MO-210 variations AL, AN (AN terminal pattern uses A1, A11, N1, N11 locations))											
	1	2	3	4	5	6	7	8	9	10	11
		1	2	3	4	5	6	7	8	9	
<b>A</b>	NC <sup>1</sup>	LBDQ	VSS	VPP				ZQ	VSS	LBDQS	NC <sup>1</sup>
<b>B</b>		VDD	VDDQ	DQ2				DQ3	VDDQ	VDD	
<b>C</b>		VSS	DQ0	DQS <sub>t</sub>				DM <sub>n</sub> <sup>3</sup> TDQS <sub>t</sub> <sup>3</sup>	DQ1	VSS	
<b>D</b>		VDDQ	VSS	DQS <sub>c</sub>				TDQS <sub>c</sub> <sup>2</sup>	VSS	VDDQ	
<b>E</b>		VDD	DQ4 <sup>4</sup>	DQ6 <sup>4</sup>				DQ7 <sup>4</sup>	DQ5 <sup>4</sup>	VDD	
<b>F</b>		VSS	VDDQ	VSS				VSS	VDDQ	VSS	
<b>G</b>		CA_ODT	MIR	VDD				CK <sub>t</sub>	VDDQ	TEN <sup>5</sup>	
<b>H</b>		ALERT <sub>n</sub>	VSS	CS <sub>n</sub>				CK <sub>c</sub>	VSS	VDD	
<b>J</b>		VDDQ	CA4	CA0				CA1	CA5	VDDQ	
<b>K</b>		VDD	CA6	CA2				CA3	CA7	VDD	
<b>L</b>		VDDQ	VSS	CA8				CA9	VSS	VDDQ	
<b>M</b>		CA1	CA10	CA12				CA13	CA11	RESET <sub>n</sub>	
<b>N</b>	NC <sup>1</sup>	VDD	VSS	VDD				VPP	VSS	VDD	NC <sup>1</sup>

NOTE 1 These balls are mechanical support balls for wide SDRAM packages.  
 NOTE 2 TDQS<sub>c</sub> is not valid on x4 based SDRAM components.  
 NOTE 3 DM<sub>n</sub> and TDQS<sub>t</sub> are not valid on x4 based SDRAM components.  
 NOTE 4 DQ4, DQ5, DQ6, and DQ7 are not valid for x4 based SDRAM components.  
 NOTE 5 TEN must be tied low (VSS).

### 5.1 Component Types and Placement

Components shall be positioned on the PCB to meet the minimum and maximum trace lengths required for DDR5 SDRAM signals.

PMIC and inductors are placed on the secondary side of the PCB. The Hub is placed on the secondary side of the PCB for raw cards not using the PMIC5030; and placed on the primary side of the PCB when PMIC5030 is placed on the raw card. See Annex and reference raw card for placement.

RCD and Temperature Sensors are placed on the primary side of RDIMM form factors except the RDIMM 1Rx8, which has Temperature Sensors on the secondary side.

## 5.2 Bulk and Distributed Decoupling Capacitance Guidelines

**Table 8 — Registered DIMM Decoupling Capacitor Guidelines**

Signal	Guideline	Notes
VIN_BULK VIN_MGMT	Reference JESD301-1, JESD301-4, JESD301-5	
VDD	Distributed capacitance around SDRAM should be such that impedance profile is met at each device.	See individual Annex Standard <b>Error! Reference source not found.</b> for impedance profile threshold.
	Bulk capacitance, reference PMIC standard	Capacitance at PMIC SWx output.
VDDQ	Distributed capacitance around SDRAM and RCD should be such that impedance profile is met at each device.	See individual Annex Standard <b>Error! Reference source not found.</b> for impedance profile threshold.
	Bulk capacitance, reference PMIC standard.	Capacitance at PMIC SWx output.
VPP	Distributed capacitance around SDRAM should be such that impedance profile is met at each device.	See individual Annex Standard <b>Error! Reference source not found.</b> for impedance profile threshold.
	Bulk capacitance, reference PMIC standard.	Capacitance at PMIC SWx output.
1.8V LDO 1.0V LDO	Reference respective JESD standards for each active component.	Individual Annex Standards will identify quantity, value, size, and location of placement.
NOTE 1 Total distributed decoupling capacitor values may vary by DIMM and may be staggered to achieve best overall impedance vs frequency response.		
NOTE 2 Bypass capacitors for DDR5 SDRAM devices are best located near the device power pins.		
NOTE 3 Depending on the SDRAM package size, capacitor placements may vary from raw card registration.		

## 6 DIMM Design Details

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### 6.1 Signal Groups

This standard categorizes DDR5 SDRAM timing-critical signals into specific groups. Figure 2 — (Example) RDIMM 2Rx4 Topology summarizes the high-speed signal groups for RDIMM. Signal groups, except Data and Strobe, implement a fly-by topology. Actual signal names in Annex may vary from individual reference design. The signal groups are:

#### Pre-RCD

- Pre-RCD CA and CS group includes: DCA[6:0]\_[B:A], DCS[1:0]\_[B:A]\_n, DPAR\_[B:A]
- Pre-RCD Clock group includes: DCK\_t and DCK\_c
- Pre-RCD Other group includes: ALERT\_n, DRST\_n
- Pre-RCD Loopback group includes: DLBDQ\_[B:A], DLBDQS\_[B:A]

#### Post-RCD to SDRAM

- Post-RCD CA group includes Q[B:A]CA[13:0]\_[B:A]
- Post-RCD CS group includes Q[B:A]CS[1:0]\_[B:A]\_n
- Post-RCD Clock group includes Q[D:A]CK\_[B:A]\_t, Q[D:A]CK\_[B:A]\_c
- Post-RCD Other group includes QRST\_[B:A]\_n, DERROR\_[B:A]\_n
- Post-RCD Other group includes QLBDQ\_[B:A], QLBDQS\_[B:A]

DQ and DQS - edge connector pin to SDRAM with series resistor

#### SideBand

- Host to Hub group: HSDA, HSCL, HSA
- Hub local bus group: LSDA, LSCL (star topology from Hub)

6.1 Signal Groups (cont'd)

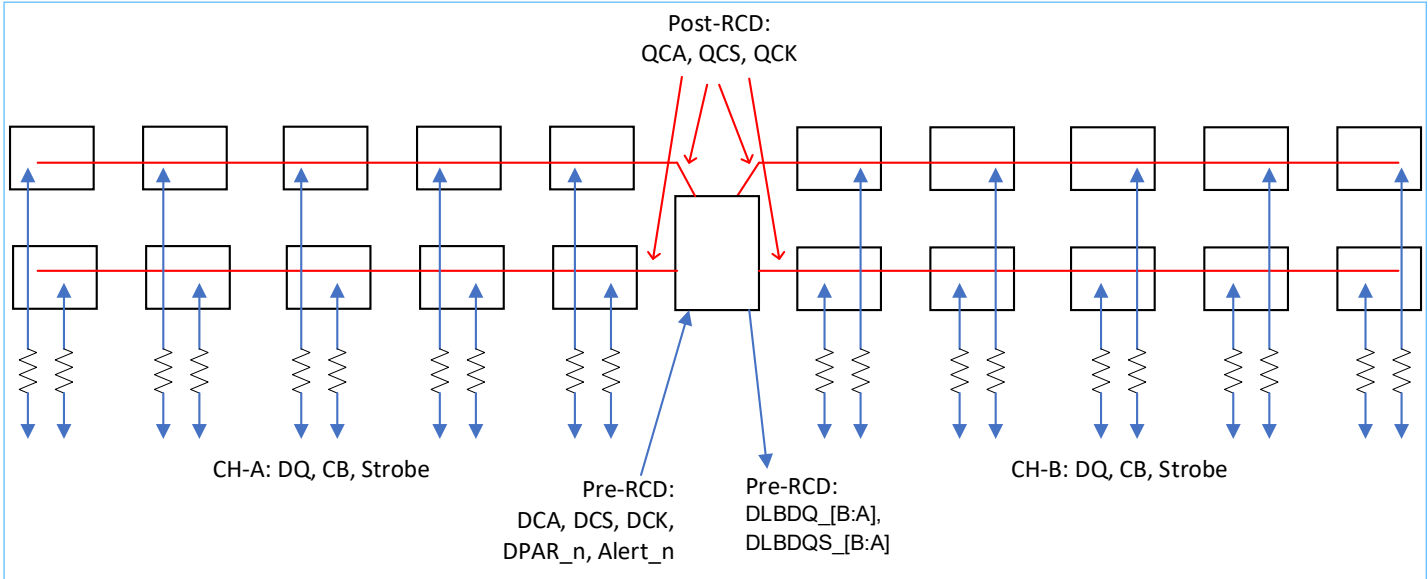


Figure 2 — (Example) RDIMM 2Rx4 Topology

## 6.2 General Net Structure Routing Rules

The usual design process should be followed to develop an adequate design. Simulations are typically required, and timing budgets considered to verify adequate performance. Documenting line lengths alone does not ensure another design using those same line lengths will meet the intended speed. This is because there are parameters that are not documented that affect the design such as vias, length of the via path, routing layers used and how the actual line lengths fall within the minimum and maximum line length range. The design goal is to specify a tight range for a specific bus that has a well-controlled time relationship to the other critical signals, e.g., QCA to QClock.

The approach to documenting DDR5 DIMM timing will be primarily simulation based for buses. Small groups of signals may be documented in terms of length only e.g., DERROR\_n, QRST\_n. A signal in each group will be documented in terms of length. Through simulation the other signals in the group will be adjusted such that the timing skew of the group is less than a specified number. This number will be identified and documented for each signal group.

The skew number is not a goal but merely the result of the design effort that produces a DIMM meeting the intended speed.

Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace segment length table that defines the length for the selected signal of the group. The Annex Standard will provide specific information for each signal group within the raw card design.

The remainder of this section provides a general overview of DDR5 net structure concepts and documents the routing rules to be followed in the design of the DDR5 DIMMs.

To use simulation almost exclusively, some conditions must be defined so that the same conclusion is reached using different simulation tools. See Table 9 for a definition of the simulation environment.

**Table 9 — Simulation Conditions**

Group	Parameter	Condition
<b>Data</b>	Motherboard Length	100 mm
	Motherboard Impedance	35 $\Omega$ (68 $\Omega$ differential for Strokes)
	Motherboard Configuration	One DIMM slot
	Routing Type	Stripline (Micro-strip)
	Driver	34 $\Omega$ with SDRAM package
<b>Pre-RCD Addr/Cmnd, Ctrl</b>	Motherboard Length	100 mm
	Motherboard Impedance	50 $\Omega$ (single ended)
	Motherboard Configuration	One DIMM per channel
	Driver	34 $\Omega$ with SDRAM package
<b>Pre-RCD Clock</b>	Motherboard Length	100 mm
	Motherboard Impedance	50 $\Omega$ differential
	Motherboard Configuration	One DIMM per channel
	Driver	34 $\Omega$ with SDRAM package
<b>Post-RCD ADD/CMD</b>	Driver	Registered Clock Driver
<b>Post-RCD CTRL</b>	Driver	Registered Clock Driver
<b>Post-RCD CK<sup>2</sup></b>	Driver	Registered Clock Driver
NOTE 1 Any deviations from these conditions must be documented in the respective Annex Standards.		
NOTE 2 Typically, these groups will be documented using length.		

6.2.1 Pre-RCD Command, Address, Chip Select, and Parity

All signals except clock can be taken as a group within each channel since loading and signal rate are the same across CA, CS\_n and Parity. Clock will be documented separately based on being routed as a differential pair.

Simulations should be done under typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one zero pattern should be used. Only steady state conditions should be included. To do this remove the first several clock periods. Remove the first five cycles if uncertain. For this group, VDD/2 should be used as the threshold for determining skew. Measure the time between the first and last crossing of VDD/2 of signals in the group. This is the skew to be documented.

Figure 3 — Pre\_RCD CA, CS Topology Example illustrates the topology for Pre-RCD CA and CS. It will be used in conjunction with Table 10 — Pre-RCD CA, CS, and Parity Length Definition Example to define the timing requirements for this group.

In this example, Address 0 is chosen as the net to be defined by length. All other signals will be adjusted in length such that the length skew is met.

Actual skew value is to be determined by the respective reference design sponsor.

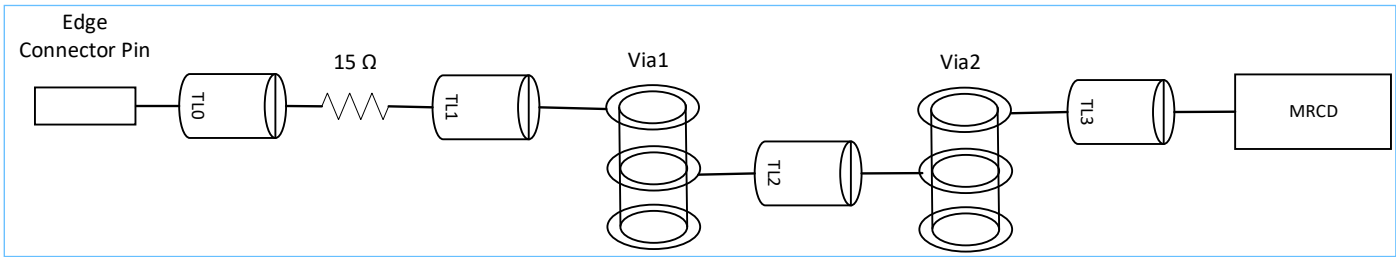


Figure 3 — Pre\_RCD CA, CS Topology Example

Table 10 — Pre-RCD CA, CS, and Parity Length Definition Example

Signal	TL0	TL1	TL2	TL3	TL0+TL1+TL2+TL3 (Compensated <sup>5</sup> )
DCA0_A	2.7	1.0	6.9	0.5	10.7
DCA0_B	2.7	0.4	7.4	.5	10.7

NOTE 1 DIMM vendor may adjust TL0 or TL1 length to accommodate component pin pitch and pad size discrepancy with reference design

NOTE 2 Signal DCA0\_[B:A] may be anywhere within the timing skew

NOTE 3 Compensated tolerance length is ± 1.00 mm excluding pin pitch adjustment

NOTE 4 Compensation = (TL0 + TL1 + TL3)/1.1 + Via1 + TL2 + Via2

NOTE 5 See section 6.6 for Compensation

NOTE 6 Compensated length for CA is ≤ 12.5 mm

NOTE 7 Compensated length for CS\_n is ≤ [CA]max + 3.0 mm

NOTE 8 Match Sub-channel A CA signal group and Sub-channel B CA signal group lengths to within 0.3 mm

NOTE 9 Match Sub-channel A CS\_n signal group and Sub-channel B CS\_n signal group lengths to within 0.3 mm

6.2.2 Pre-RCD Clock

Clock is routed as differential pair.

Figure 4 illustrates the topology for the Pre-RCD Clock. It will be used in conjunction with Table 11 to define the requirements for this group. Since it is a single signal a length tolerance is not required, and length alone will be used

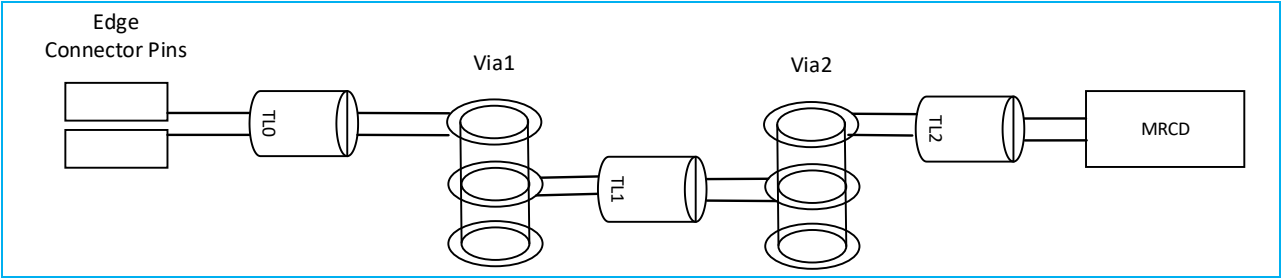


Figure 4 — Pre-RCD Clock Topology Example

Table 11 — Pre-RCD Clock

Signal	TL0	TL1	TL2	TL0+TL1+TL2 Compensated
CK_t	2.2	5.0	0.5	7.5
CK_c	2.2	5.0	0.5	7.5

NOTE 1 CK\_t and CK\_c compensated length to be within 0.1 mm

NOTE 2 Compensation = (TL0 + TL2)/1.1 + Via1 + TL1 + Via2

NOTE 3 See clause 6.6 for Compensation

6.2.3 Post-RCD Clock, Control, Address and Command Signal Groups

The DDR5 DIMMs implement a fly-by topology for routing CK, CA, and CS\_n signal groups independently for Channel A and Channel B. Each group, CK, CA, and CS\_n, will be documented separately. This division is based on possible loading differences.

6.2.4 Post-RCD Command and Address Signal Group

Loading differences require the CA group to be treated separately from the Clock and CS\_n groups. The CA group is further divided into RCD outputs of left side (Channel A) and right side (Channel B) group. Document the length of one signal in each group per Channel per RCD output. Use simulation to match the timing of the group to be within a defined skew.

Simulations should be done under typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this remove the first several clock periods. Remove the first five cycles if uncertain. VDD/2 should be used by this group as the threshold to determine skew. Where there are multiple ranks, rank 0 will be used to define skew. All rank 0 SDRAM locations must be evaluated separately. The maximum skew for all rank 0 SDRAMs is to be the skew documented. One method is graphical, where all signals for a group at one SDRAM are plotted. Measure the time between the first and last signal crossing VDD/2. This is the skew for this SDRAM. Repeat this for each rank 0 SDRAM on each Channel. The maximum is the skew to be documented.

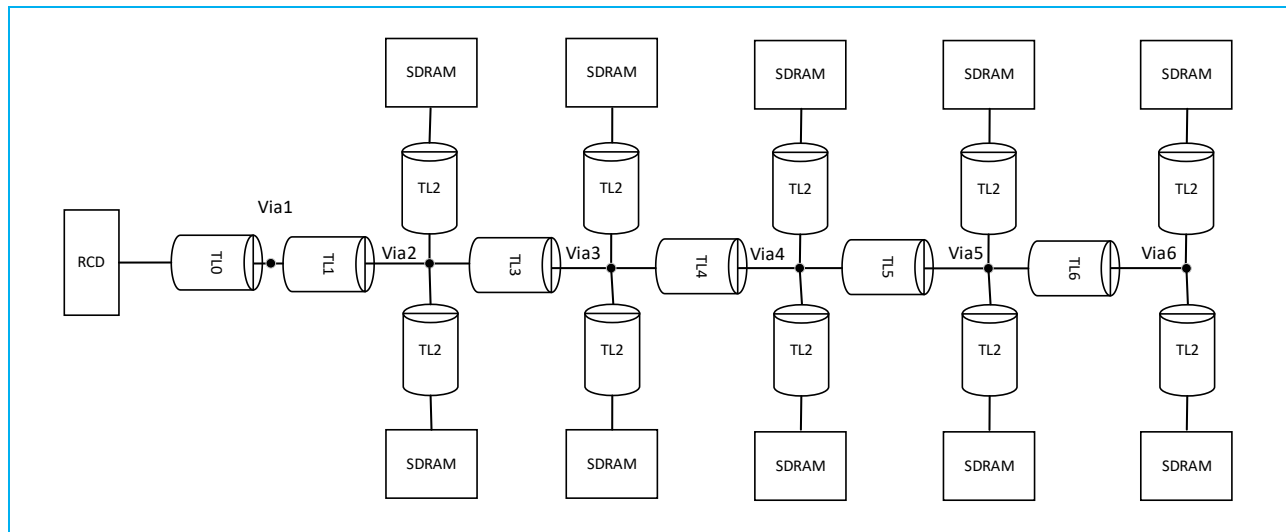


## 6.2.4 Post-RCD Command and Address Signal Group (cont'd)

Actual skew value is to be determined by the respective reference design sponsor. The skew is to be documented.

Figure 5 illustrates a topology example for the Post-RCD CA. It will be used in conjunction with Table 12 to define the timing requirements for this group.

TL2 is not used in compensation method if length is the same for all signals at all SDRAM pin locations.



**Figure 5 — Post-RCD QCA Daisy-Chain Topology Example**

**Table 12 — Post-RCD CA Daisy Chain Length Definition Example**

Signal	TL0 (MS)	TL1 (SL)	TL3 (SL)	TL4 (SL)	TL5 (SL)	TL6 (SL)	TL2 (MS)
QACA0_A	0.5	15.5	13.0	13.0	13.0	13.0	0.6
QBCA0_A	0.5	23.8	13.0	13.0	13.0	13.0	0.6
QACA0_B	0.5	15.6	13.0	13.0	13.0	13.0	0.6
QBCA0_B	0.5	23.9	13.0	13.0	13.0	13.0	0.6

NOTE 1 Signal QxCAX\_x may be anywhere within the timing skew at each SDRAM.

NOTE 2 TL3, TL4, TL5, TL6 may be of same segment length

NOTE 3 Via = Via length travel, add layer change from TL0 to TL1, add if signals change layers between SDRAM.

NOTE 4 Compensated tolerance length is  $\pm 1.00$  mm

NOTE 5 Compensation D0 =  $TL0/1.1 + Via1 + TL1$

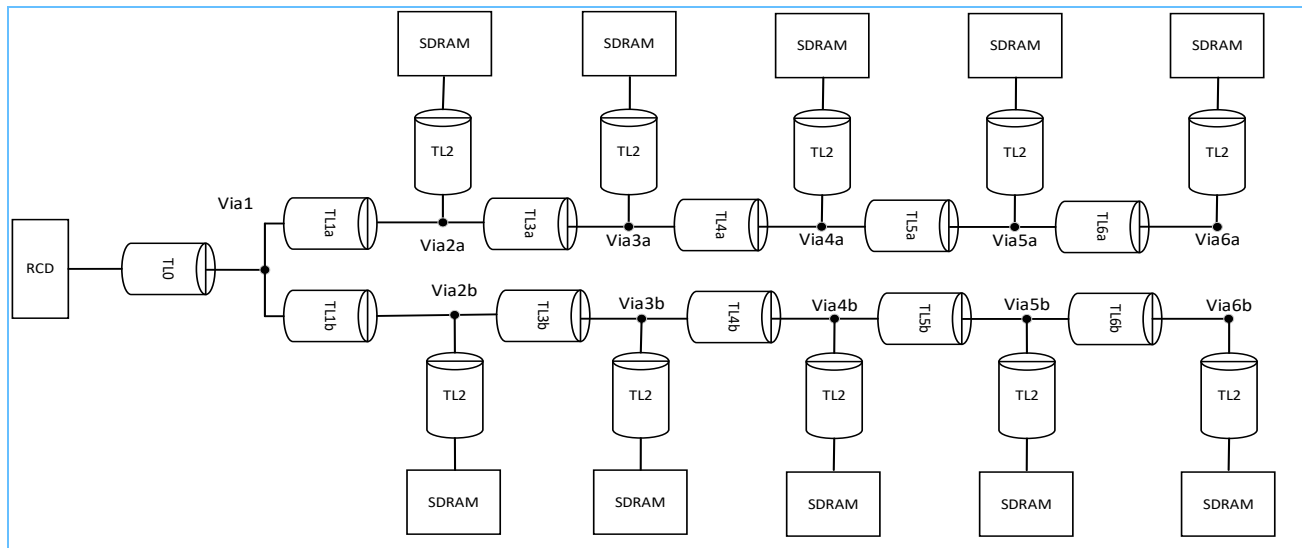
NOTE 6 Compensation D1 =  $TL0/1.1 + Via1 + TL1 + TL3$

NOTE 7 Compensation D2 =  $TL0/1.1 + Via1 + TL1 + TL3 + TL4$

NOTE 8 Compensation D3 =  $TL0/1.1 + Via1 + TL1 + TL3 + TL4 + TL5$

NOTE 9 Compensation D4 =  $TL0/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6$

## 6.2.4 Post-RCD Command and Address Signal Group (cont'd)



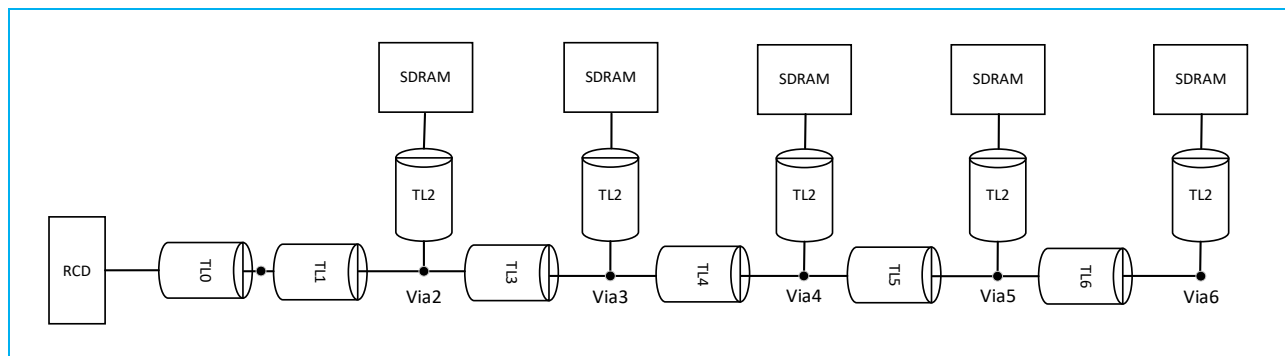
**Figure 6 — Post-RCD QCA Topology for 8000 Mbps and Higher**

Raw Cards for 8000 Mbps and higher use the “Y” topology for improved Address/Command signaling. See Annex and Raw Card for specific details.

## 6.2.5 Post-RCD Control Signal Group

This group will use the same approach as the Post-RCD CA Group. Clock and CS will be documented in the Annex Standard separately when loading is different. Clock and Control segment length will be designed to align with CA and will be defined in each raw card Annex. Refer to the Post-RCD CA clause 6.2.4 for details.

Match Clock<sub>t</sub> and Clock<sub>c</sub> TL<sub>x</sub> segments to be within 0.1 mm. Match Clock<sub>t</sub> and Clock<sub>c</sub> compensated overall length to be within 0.1 mm.

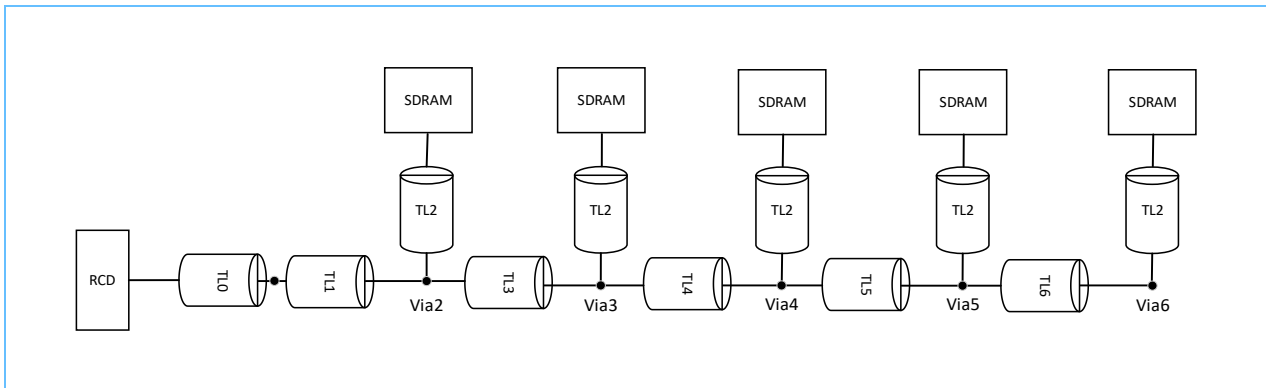


**Figure 7 — Post-RCD QCS<sub>n</sub> Daisy-Chain Topology Example**

## 6.2.6 Post-RCD Clock Signal Group

Post-RCD clocks for raw cards 7200 Mbps and less will use the same approach as the Post-RCD CA Group. Clock segment length will be designed to align with CA and will be defined in each raw card Annex. Refer to the Post-RCD CA section for details.

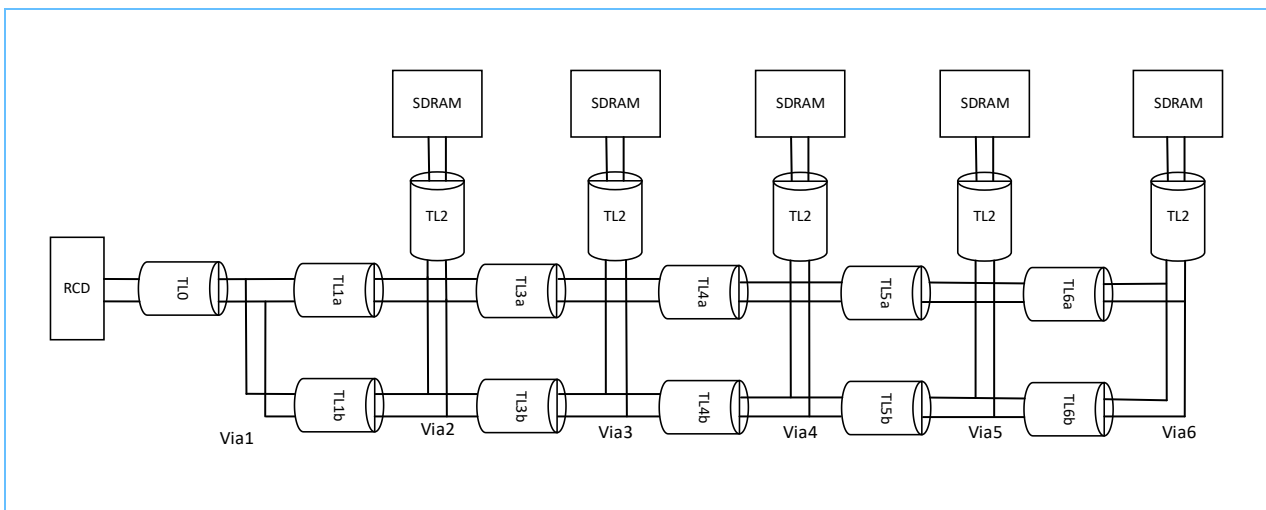
Match Clock<sub>t</sub> and Clock<sub>c</sub> TLx segments to within 0.1 mm. Match Clock<sub>t</sub> and Clock compensated overall length to be within 0.1 mm.



**Figure 8 — Post-RCD QCK Daisy-Chain Topology for Raw Cards through 7200 Mbps**

Post-RCD clocks for raw cards targeting 8000 to 9200 Mbps use a twin-clock topology approach. Clock segment length will be designed to align with CA and will be defined in each raw card Annex. Refer to the Post-RCD CA section for details.

Match Clock<sub>t</sub> and Clock<sub>c</sub> TLx segments to within 0.1 mm. Match Clock<sub>t</sub> and Clock compensated overall length to be within 0.1mm.



**Figure 9 — Post-RCD QCK Twin-Clock Topology for 8000 to 9200 Mbps Raw Cards**

## 6.2.7 Data and Strobe Signal Group

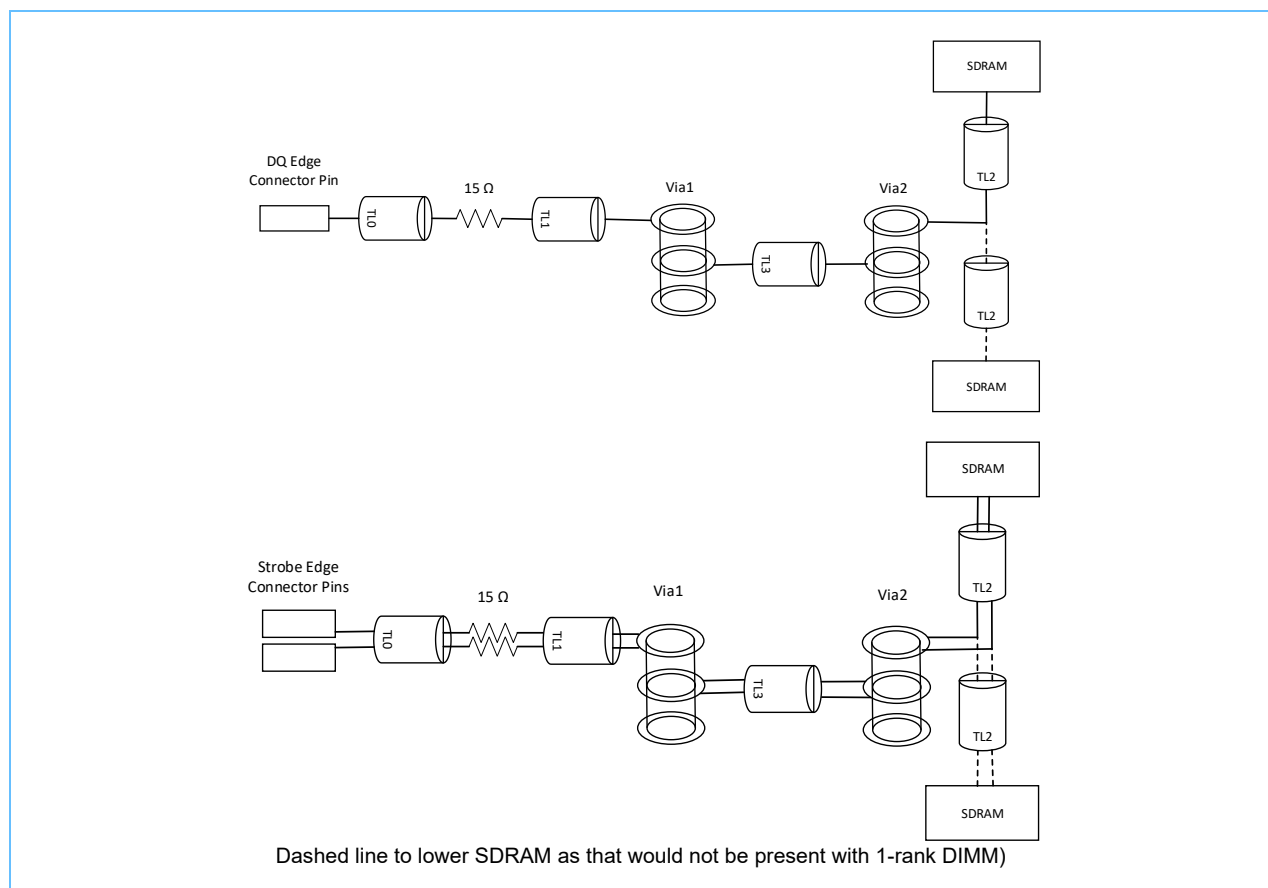
This group contains the Data, Checkbits, and Strobe signals. RDIMM raw cards can use x4 or x8 SDRAM.

There are 9 (EC4) or 10 (EC8) subgroups per Channel that are identified based on each strobe with half the Data bits coming from each side of the DIMM edge fingers to each SDRAM. Each subgroup (4 Data or 8 Data, and a strobe pair) will be called a lane. Each lane for a x4 SDRAM is also known as a nibble. Each lane for a x8 SDRAM is known as a byte. The Strobe for each lane will be routed differentially and documented using length. One Data net within each lane will be documented in length. A timing skew will be documented for each lane. Skew will be applied to each lane separately. Each lane may have different timing. illustrates Data topologies. depicts an example for Data, Checkbits, and Strobe definition.

Actual skew value is to be determined by the respective reference design sponsor.

Simulations should be done under typical conditions. This is to be an uncoupled simulation. Crosstalk is to be ignored. An alternating one-zero pattern should be used. Only steady state conditions should be included. To do this, remove the first several clock periods. Remove the first five cycles if uncertain. For this group, a threshold is determined by looking at the cross point of the rising and falling edges in an eye pattern. Select a threshold that would provide the smallest skew. Where there are multiple ranks, only evaluate the timing for SDRAMs making up rank 0. Measure the time between the first and last signal crossing. This is the skew for this lane. Repeat this for each lane. The maximum skew for each lane is to be documented.

Strobe is not included in the skew measurement.



**Figure 10 — Data and Strobe Diagram Example**

### 6.2.7 Data and Strobe Signal Group (cont'd)

### Table 13 — Example of 2Rx4 DQ/Strobe Lengths

Signal	TL0 (ms)	TL1 (ms)	TL2 (sl)	TL3 (ms)	TL0+TL1+TL2 (Compensated)	Bus
DQS0_A_t, DQS0_A_c	3.2	0.8	7.1	1.8	11.8	-
DQ0_A	3.1	0.7	5.5	0.6	10.0	DQ[3:0]_A
DQS5_A_t, DQS5_A_c	3.2	0.8	18.9	1.8	23.5	-
DQ4_A	2.9	0.8	18.4	0.6	22.8	DQ[7:4]_A
...						
DQS4_A_t, DQS4_A_c	3.2	0.8	9.5	1.8	14.2	-
CB0_A	3.2	0.8	12.2	0.6	16.8	CB[3:0]_A
DQS9_A_t, DQS9_A_c	3.2	0.8	19.5	1.8	24.1	
CB4_A	2.9	0.8	17.9	0.6	22.3	CB[4:7]_A
		Channel B will have a similar table for Data, Checkbits and Strobe.				

NOTE 1 DIMM vendor may adjust TL0 or TL1 length to accommodate component pin pitch and pad size discrepancy with reference design

NOTE 2 Match DQS\_t and DQS\_c TL0 segments to be within 0.1 mm, and overall compensated length to be within 0.1 mm

NOTE 3 Signal DQx\_[B:A] may be anywhere within the timing skew

NOTE 4 Compensated tolerance length is  $\pm 1.00$  mm

NOTE 5 Compensation

- 2-rank RDIMM –  $(TL0 + TL1)/1.1 + Via1 + TL3$
- 1-rank RDIMM –  $(TL0 + TL1 + TL2)/1.1 + Via1 + TL3$

NOTE 6 Compensated DQ and DQS minimum  $\geq 8.5$  mm

NOTE 7 Compensated DQ maximum  $\leq 24$  mm

NOTE 8 Compensated DQ -to- DQ Skew  $\leq 1.0$  mm

NOTE 9 Compensated DQS maximum  $\leq 27$  mm

NOTE 10 Compensated DQS -to- DQ skew  $[DQS-DQ] \leq 5.0$  mm

### 6.3 Design Rules

**Table 14 — Wiring**

	Sub-Channel-A		Sub-Channel-B	
MIR (Mirror)	Frontside SDRAM	Backside SDRAM	Frontside SDRAM	Backside SDRAM
	VSS	VDDQ	VDDQ	VSS
CA_ODT	Last SDRAM (Front/Back) from RCD	All Other SDRAM (Front/Back)	Last SDRAM (Front/Back) from RCD	All Other SDRAM (Front/Back)
	Vddq	GND	Vddq	GND
CAI	Top Row (Front/Back)	Bottom Row (Front/Back)	Top Row (Front/Back)	Bottom Row (Front/Back)
	VDDQ	VSS	VDDQ	VSS
TEN	All SDRAM	VSS	All SDRAM	VSS
QCA	2Rx4	Top Upper A (AB-CA/CS0,CK0B) B (BB-CA/CS0,CK1B)	Bottom Upper A (AB-CA/CS1,CK0D) B (BB-CA/CS1,CK1D)	
		Top Lower A (AA-CA/CS0,CK0A) B (BA-CA/CS0,CK1A)	Bottom Lower A (AA-CA/CS1,CK0C) B (BA-CA/CS1,CK1C)	
	1Rx4	Top A (AA-CA/CS0,CK0A) B (BA-CA/CS0,CK1A)	Bottom A (AACA,ABCS0,CK0C) B (BACA,BBCS0,CK1C)	
	2Rx8	Top A (AA-CA/CS0,CK0A) B (BA-CA/CS0,CK1A)	Bottom A (AA-CA/CS1,CK0C) B (BA-CA/CS1,CK1C)	
	1Rx8	Top/Bottom A (AA-CA/CS0,CK0A) Gen 0,1 A (AA-CA/CS0,CK0C) Gen 2	Top/Bottom B (BA-CA/CS0,CK0A) Gen 0,1 B (BA-CA/CS0,CK0C) Gen 2	
VR_OE	Signal pin with PMIC5030. Raw cards using PMIC5030 will tie this pin through 200k ohm series pull up resistor to VIN_BULK.			
A13	If “MIR” pin tied to GND – A13 to A13, A12 to A12 If “MIR” pin tied to VDDQ – A13 to A12, A12 to A13			
NC/NU/RFU Pins	SDRAM - Not connected (Floating)			
	PMIC - GND corner pins. For all others, check with vendor			
LoopBack Data/Strobe	Each channel has a daisy chain from RCD through SDRAM. 2 row designs start at lower row SDRAM and continue through upper row ending with SDRAM closest to RCD			
DCS1	Must be routed to RCD for all RDIMM raw cards.			
SDRAM	See Annex for Raw Card revision maximum package size. Nominal package (10.0x11.0) mm, Maximum package (10.1x11.1) mm Nominal package (10.0x11.7) mm, Maximum package (10.1x11.8) mm			
DIMM Outline	The raw card outline is compliant with MO-329.			
Via	<ul style="list-style-type: none"> <li>- Signal vias must not be placed close together (except differential signals). Recommended to place power or GND via between Signal vias.</li> <li>- Signal vias under SDRAM are not to be placed vertically or horizontally adjacent in BGA grid.</li> <li>- 0.200 (Drill) / 0.400 (pad) / 0.600 (anti-pad) mm is standard size</li> </ul>			

**Table 14 — Wiring (cont'd)**

	<b>Sub-Channel-A</b>		<b>Sub-Channel-B</b>
<b>Component Pads</b>	Pads for all components are left to the reference card designer to define. DIMM Supplier may adjust.		
<b>Inductor Area</b>	Remove via and plane shapes/traces in between inductor pads on surface layer		
<b>Temperature Sensor Location</b>	See Annex for location and address strapping. TS01 is placed on Channel-A side. TS00 is placed on Channel-B side.		
<b>Hub location</b>	Place on secondary side above PMIC. If place in different location the Annex should identify in deviation section.		
<b>BGA Pad Size</b>	SDRAM	0.350 mm	DIMM Supplier may adjust.
	RCD, TS	0.270 mm	DIMM Supplier may adjust.
<b>Inductor pads</b>	No traces or vias to be routed between inductor pads on outer layers. Signals are not to be routed under inductor pads on Ln-1. Signals routed under inductor pads to have at least one full plane layer between.		
<b>Outline upper side notches</b>	Sponsored raw card outline to contain these upper notches. DIMM vendor can determine whether to include or not in product.		

### 6.3 Design Rules (cont'd)

**Table 15 — Circuit Requirements**

SideBand Bus		LDO 1.8V	LDO 1.0V	Place near device pin
	Hub Capacitor	1.0 μF	1.0 μF	
	PMIC Capacitor	0.1 μF 4.7 μF	0.1 μF 4.7 μF	
	RCD Capacitor	n/a	0.1 μF	
	TS[01,00] Capacitor	0.1 μF	0.1 μF	
Copper voiding under edge pins on L2 and Ln-1		Refer to raw card artwork. Copper voiding scheme instantiated to improve signal integrity.		
Via breakout pattern under SDRAM		Signal vias should not be placed in adjacent vertical and horizontal position except differential signals. Recommended to place power or GND Via between Signal Vias. Improved cross talk isolation.		
1-Rank DIMM unused Clock and Chipselect		Unused clock T and C and CS1_n signals to be terminated with 33 ohm resistor to Vddq.		
Signal Group Length Rules	DCA max (Addr[6:0, PAR)	≤ 12.5 <sup>1</sup> mm ≤ 11.5 <sup>2</sup> mm	Match C/A signals within a subchannel to ± 0.1 mm. Match subchannel A and B DCA signal groups to ± 0.3 mm <sup>1</sup> , ± 3.0 mm <sup>2</sup> .	
	Chipselect (DCS)	DCS ≤ 14.5 mm <sup>1</sup> DCS ≤ DCA max + 3.0 mm <sup>2</sup>	Match subchannel A and B DCS_n signals to ± 0.3 mm <sup>1</sup> , ± 3.0 mm <sup>2</sup> ..	
	DCK_t/c	≤ 12.5 <sup>1</sup> mm ≤ 11.0 <sup>2</sup> mm	Match subchannel A and B DCK signals to ± 0.3 mm <sup>1</sup> ., +/- 1.5 mm <sup>2</sup> Match each DCK _t and _c TLx segments to be within 0.1 mm.	
	DQ/DQS min	8.5 ≤ mm		
	DQ max	≤ 24 mm		
	DQ – DQ Skew	≤ 1.0 mm	Skew applies to either Nibble (x4 module), or Byte (x8 module).	
	DQS max	≤ 27 mm		
	DQS – DQ Skew	[DQS-DQ] ≤ 5.0 mm	Skew applies to either Nibble (x4 module), or Byte (x8 module). It is preferred that DQS is shorter than DQ.	
Series Resistor	DQ / Strobe	15 Ω	Place close to edge finger	
	Pre-RCD - Addr/Cmnd/Ctrl	15 Ω	Pre-RCD, place close to edge finger	
	PCAMP	249 Ω	249 ohm, 1/10W, 0603 series resistor placed near edge connector pin.	
DQ, DQS, Address, Command, Control, Parity, Clock		Signals to reference ground (GND / VSS)		
Edge Finger Pin-1 Capacitor	VIN_BULK	(1) 10 μF 0603	Applies to all raw cards for RDIMMs near edge connector pins.	
	VIN_MGMT	(1) 4.7 μF 0402		
NOTE 1 7200 Mbps and below NOTE 2 8000 Mbps and above				



## 6.3 Design Rules (cont'd)

**Table 16 — Spacing Rules**

<p>These are the spacing rules for raw card copper features including keepout requirements. Violations of the Rules are to be noted in the Annex for the specific raw card. It is preferred that additional details be included to identify the areas of the violations. These rules are for design of the reference card only. It is not required that these rules be met by individual manufacturers building from the reference designs. These design rules are intended to be used for the reference RDIMM designs submitted to JEDEC for ballot. RDIMMs manufactured from the reference designs may use modified rules by the RDIMM Supplier to support their manufacturing process.</p>			
Category	Item	Value (mm)	
Spacing	copper to copper (Outer/Inner)	0.075 / 0.070	
	Pad to pad (For pads of different components that are soldered down)	0.200	
	Line to (N)SMD pad (12 V / the others)	0.113 / 0.100	
	Line to line (Single / Diff pair)	0.100 / 0.090	
	Line to Shape	0.125	Where impedance is important, use the 0.20 rule.
	Shape to Shape	0.100	
	Via (pad) to NSMD pad (12 V / the others / same Net)	0.113 / 0.100 / 0.100	
	Via (pad) to SMD pad (12 V / the others / same Net)	0.113 / 0.100 / 0.020	
	Via (pad) to Via (pad)	0.125	
	Via (pad) to Line (Outer/Inner)	0.09 / 0.07	
	Drill wall to Board edge (nominal)	0.450	Nominal board edge and drill being centered in pad
Comp to Comp	IC to IC (max. PKG size)	0.250	Inductor is assumed IC. (Max PKG size 4.3 mm)
	IC (max.) to Passive (nominal)	0.250	
	Passive to Passive (nominal PKG size)	0.250	
Copper Keepout	Board top edge (nom) to copper	0.250	
Component Keepout	DIMM w/o HS - Top edge of board to Passive (max.) or IC (max.)	0.300	Nominal board edge and package body max. size criteria
	DIMM w/ HS - Top edge of board to Passive (max.) or IC (max.)	TBD	
Traces	Outer Layer Trace Width (minimum)	0.07	
	Inner Layer Trace Width (minimum)	0.05	

## 6.4 Impedance Target

The impedances defined here are the RDIMM reference design targets.

Single ended  $> 40 \Omega \pm 10\%$

Single ended  $\leq 40 \Omega \pm 4$  ohms

Single ended 20 and 25  $\Omega \pm 4$  ohms

The differential signal pair (clock and strobe) trace targets are routed with the single ended traces defined above with 0.100mm space (nominal). DIMM vendors may adjust to optimize design.

**Table 17 — Impedance Targets**

Signal (Raw Card)	4800-5600 (A,C,D,E)	6400 - 7200 (A,C,D,E)	8000 - 9200 (A,C,D,E)
DQ/DM (pre-resistor)	35	35	35
DQR/DMR (post-resistor)	35	35	35
DCA	50	50	50
QCA	50	50	40
DCS	50	50	50
QCS	50	50	40
Parity	50	50	50
ALERT_n	50	50	50
RESET_n	50	50	50
DERROR_IN_n	50	50	50
QRESET_n	50	50	50
CAMP	50	50	50
HSCL, HSDA, HSA	50	50	50
LSCL, LSDA	50	50	50
LBDQ, LBDS	50	50	50 <sup>1</sup>
PWR_GOOD	-	-	-
ZQ	50	50	50
DCK	50(85)	50(85)	50(85)
QCK	25(45-50)	25(45-50)	20(40)
DQS (pre-resistor)	35(68)	35(68)	35(68)
DQSR (post-resistor)	35(68)	35(68)	35(68)
NOTE 1 Raw Card D2 reference design artwork uses 40 ohm			
NOTE 2 (Differential) signal targets are with 100 $\mu$ m spacing			

## 6.5 Rules for Compensation

### 6.5.1 Velocity

Velocity compensation for microstrip (ms) line to stripline (sl) is to divide the microstrip length by a factor of 1.1

$$SL = MS/1.1$$

### 6.5.2 Via

Via compensation is 1x the length of via barrel traveled by the signal.

## 6.6 Rules for Signal Length Calculation

Via = travel length of signal when transitioning from layer to layer. Travel can be outside layer to inside layer, or inside layer to inside layer.

### 6.6.1 DQ/Strobe (DQ, DQS)

One SDRAM Load –  $(TL0 + TL1 + TL2)/1.1 + Via1 + TL3 + Via2$

One rank x8 and one rank x4 RDIMMs include all via travel transitions.

Two SDRAM Loads –  $(TL0 + TL1)/1.1 + Via1 + TL3 + TL2/1.1$

Two rank x8 and Two rank x4 RDIMMs include via travel transition from micro-strip to strip-line after resistor and does not include via travel from stripline to micro-strip at via under the SDRAM where the micro-strip connects with SDRAM pad.

### 6.6.2 Pre-RCD (DCA, DCS)

Edge finger pin to RCD pad –  $(TL0 + TL1 + TL2)/1.1 + Via1 + Via2 + TL2$

### 6.6.3 Pre-RCD Clock

Clock\_t/c –  $(TL0 + TL2)/1.1 + Via1 + TL1 + Via2$

Since Clocks edge connector pins are on secondary side and RCD is on primary side, via travel is thickness of PCB less outer layer Cu thickness.

#### 6.6.4 Post-RCD QCA, QCS, and QCK

##### QCA

- 1st SDRAM from RCD
  - o Two SDRAM loads at each node –  $TL0/1.1 + Via1 + TL1$  (5600 Mbps and less)
  - o One SDRAM load at each node –  $(TL0 + TL2)/1.1 + Via1 + TL1 + Via2$  (6400 Mbps and higher)
- Last SDRAM from RCD
  - o Two SDRAM loads at each node –  $TL0/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6$  (5600 Mbps and less)
  - o One SDRAM load at each node –  $(TL0 + TL2)/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6 + Via2$  (6400 Mbps and higher)

##### QCS\_n

- 1st SDRAM from RCD
  - o One SDRAM load at each node –  $(TL0 + TL2)/1.1 + Via1 + TL1 + Via2$
- Last SDRAM from RCD
  - o One SDRAM load at each node –  $(TL0 + TL2)/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6 + Via2$

##### QCK\_t/c

- 1st SDRAM from RCD
  - o One SDRAM load at each node –  $(TL0 + TL2)/1.1 + Via1 + TL1 + Via2$
- Last SDRAM from RCD
  - o One SDRAM load at each node –  $(TL0 + TL2)/1.1 + Via1 + TL1 + TL3 + TL4 + TL5 + TL6 + Via2$
- TLx a/b sections are targeted to be within 0.10 mm of each other. DIMM vendors are allowed to adjust segment length of “a” vs “b” based on simulation results.
- QCK\_t/c uses twin clock topology for 8000+ Mbps raw cards. See each Annex for compensation rule applied.

## 6.7 Rules for Designs

The SDRAM package is a significant factor in the performance of RDIMM. SDRAM packages vary between manufacturers and between SDRAM die within a single company. It is challenging to create a raw card design that can accommodate all SDRAM designs that will physically fit on the RDIMM.

To increase the number of suppliers and SDRAM packages that a single reference design letter can cover, some changes to the variation that may be applied for manufacturing is defined. A design letter e.g., "A" and registration e.g., "1" as in "A1", is a single reference design. An individual manufacturer may modify the design including the trace lengths within the rules below.

### Rules for allowed variation:

1. Placement configuration must match the reference design.
2. Physical placement may be changed. There is no specific limit.
3. All routing topologies must be maintained. The lengths may be adjusted as defined for signal groups.
4. Clock routing lengths may be adjusted as needed to maintain timing to CA and CS<sub>n</sub> signals, Post RCD.
5. Control (CS<sub>n</sub>) routing lengths may be changed as needed to maintain timing to the Clock, Post RCD.
6. CA segment lengths between the SDRAMs may be adjusted by +/- 3 mm relative to the reference design.
7. CA segment lengths between the RCD and the first SDRAMs may be adjusted by +/- 10 mm.
8. Maximum skew for the CA bus at the SDRAMs must be less than or equal to the reference design. It is suggested that the skew of the reference design be simulated with the same tool that is used for the final manufactured design so that simulator differences are minimized.

## 6.8 DQ Wiring to Support CRC

DDR5 has a CRC feature that has been added to support higher speeds. Generally, when using CRC, the bit order is 1:1 between the source and the destination. This is not true for DIMMs where the bit order is somewhat random based on minimizing routing length to maximize signal integrity. The CRC computation is based on a byte. For x4 based SDRAMs the computation is truncated to 4 bits, a nibble. See DDR5 SDRAM Standard JESD79-5 for a more complete explanation of how CRC is implemented. To fix the mapping issue the host must understand the bit order at the SDRAM to map the DQ bits into the CRC generator for WRITE commands so that the SDRAM will decode the CRC correctly. The same is true for READs.

When there is more than one rank on a DIMM the even ranks are on the front and the odd ranks are on the back. When SDRAMs are placed back-to-back and are of a different package rank the DQ relationship between the even ranks and the odd ranks are fixed. To reduce the number of variations in the DQ mapping a couple of rules are defined.

Rule 1: Bits within a nibble and strobe pair must stay together.

Rule 2: Nibbles may be swapped within a byte.

Rule 3: Definition of mapping is for rank 0 only. All even ranks have the same DQ mapping. Even rank to odd rank mapping is to swap bit 0 with 1, swap bit 2 with 3, swap bit 4 with 5 and swap bit 6 with 7.

For DIMMs that use 3DS components, the rank definition applies to package ranks. The additional die within a 3DS component are logical ranks and are part of one package rank. Another way of looking at this is that each Chipselect (CS<sub>n</sub>) used is one package rank. Where there is only one package rank, that rank may be placed on the front or the back or split between the front or back.

Use of CRC is an optional feature. It is required that all reference designs support CRC. The definition for CRC can be found in the JESD79-5 Standard for DDR5 SDRAMs.

## 6.8 DQ Wiring to Support CRC (cont'd)

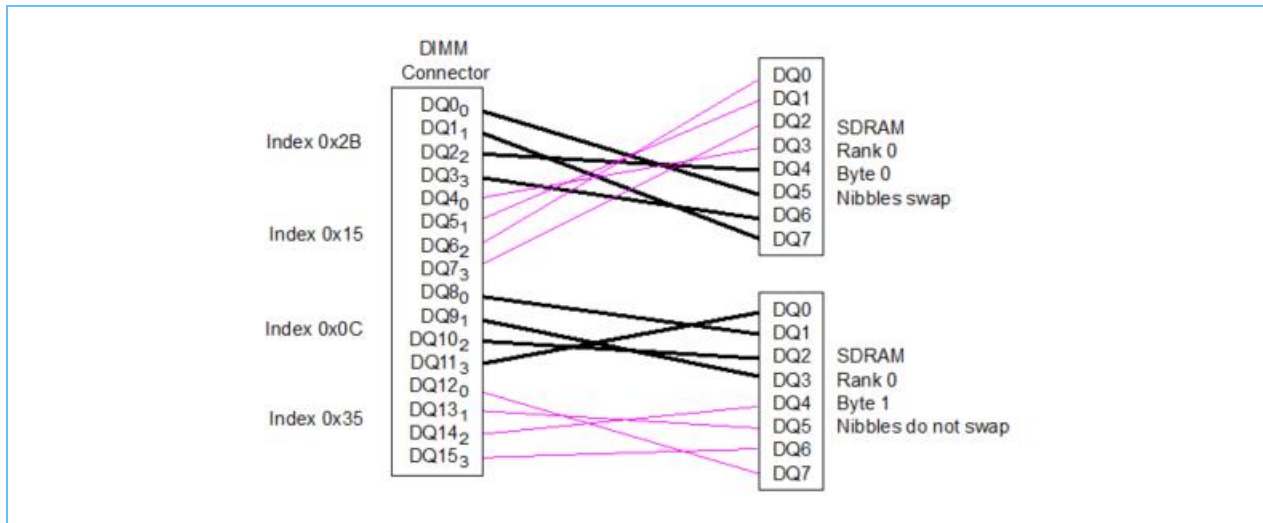


Figure 11 — Example of DQ Wiring

## 6.9 RDIMM Configuration

### 6.9.1 DIMM Connectivity Wiring

2Rx4										
DIMM Side	Row	Clock	CS	CA	Rank					
Top	Lower	QACK	QACS0	QACA	0					
Top	Upper	QBCK	QBCS0	QBCA	0					
Bottom	Lower	QCCK	QACS1	QACA	1					
Bottom	Upper	QDCK	QBCS1	QBCA	1					
2Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Top		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
Bottom	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
2Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Top	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]
Bottom		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

1Rx4										
DIMM Side	Row	Clock	CS	CA	Rank					
Top	Lower	QACK	QACS0	QACA	0					
Bottom	Lower	QCCK	QBCS0	QACA	0					
1Rx4 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[3:0]		[11:8]		[19:16]		[27:24]		CB[3:0]	
Bottom		[7:4]		[15:12]		[23:20]		[31:28]		CB[7:4]
1Rx4 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:4]		[15:12]		[23:20]		[31:28]	CB[3:0]	
Bottom	[3:0]		[11:8]		[19:16]		[27:24]			CB[7:4]

2Rx8										
DIMM Side	Row	Clock	CS	CA	Rank					
Top	Lower	QACK	QACS0	QACA	0					
Bottom	Lower	QCCK	QACS1	QACA	1					
2Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]
Bottom		[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]
2Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top		[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]
Bottom		[7:0]		[15:8]		[23:16]		[31:24]		CB[7:0]

6.9.1 DIMM Connectivity Wiring (cont'd)

1Rx8 (less than 8000 Mbps)										
DIMM Side	Row	Clock	CS	CA	Rank					
Top	Lower	QACK	QACS0	QACA	0					
Bottom	Lower	QACK	QACS0	QACA	0					
1Rx8 (8000 Mbps and Faster)										
DIMM Side	Row	Clock	CS	CA	Rank					
Top	Lower	QCCK	QACS0	QACA	0					
Bottom	Lower	QCCK	QACS0	QACA	0					
1Rx8 Sub Channel 0 (Channel A)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top			[15:8]				[31:24]			
Bottom	[7:0]				[23:16]				CB[7:0]	
1Rx8 Sub Channel 1 (Channel B)										
Side	DQS0	DQS5	DQS1	DQS6	DQS2	DQS7	DQS3	DQS8	DQS4	DQS9
	Nib 0	Nib 1	Nib 2	Nib 3	Nib 4	Nib 5	Nib 6	Nib 7	Nib 8	Nib 9
Top	[7:0]				[23:16]					
Bottom			[15:8]				[31:24]		CB[7:0]	

Figure 12 — DIMM Connectivity Wiring

6.9.2 Control Wiring

Figure 13 defines the required control wiring for two row reference designs. The Design Standard Annex will include equivalent information in a clear manner for designs not covered in Figure 13.

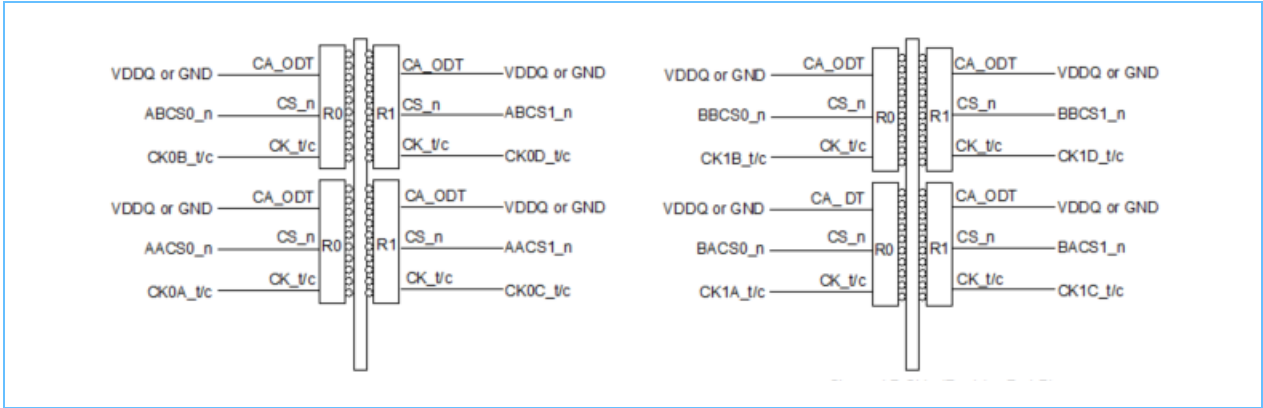


Figure 13 — DDR5 2Rx4 (Planar/3DS) Control Wiring



### 6.9.3 ALERT\_n Circuit Wiring

DERROR\_n will be wired as a long fly-by connection with the RCD at one end. Connection will be from the ERROR\_n pin of the RCD to the SDRAM ALERT\_n pin of each in a daisy chain manner for each channel. There will be a pull-up resistor to VDDQ at the end farthest SDRAM electrically from the register for each Channel. There will be a filter capacitor near the RCD pin for each channel. This circuit should be simulated to verify clean signal edges. Figure 14 demonstrates one possible wiring for this circuit.

Terminate DERROR\_n with 47  $\Omega$  near last SDRAM of daisy chain of each Channel.

Place 10 pF near RCD of each Channel

The ALERT\_n output of the RCD is connected to the ALERT\_n pin of the edge pin connector.

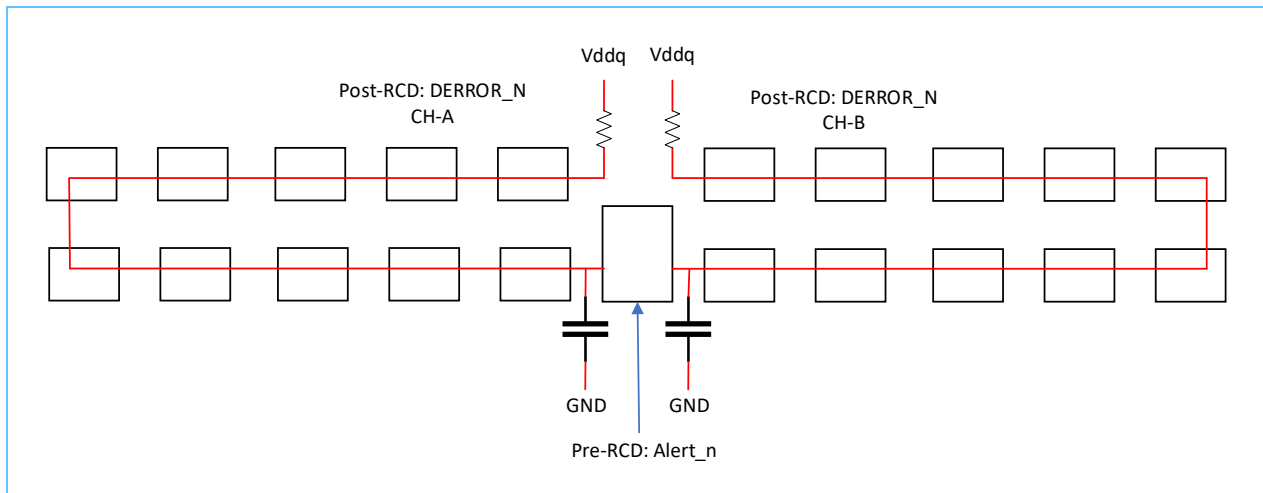
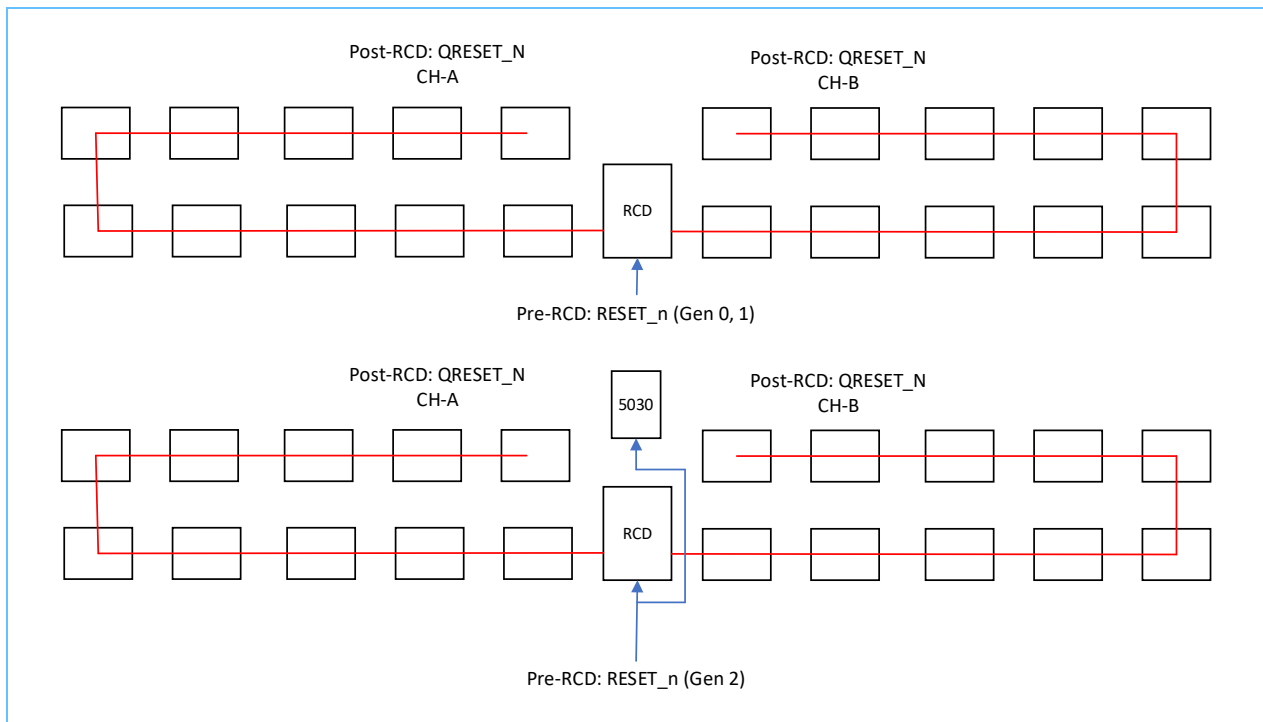


Figure 14 — Example Wiring of the ALERT\_n, DERROR\_n

### 6.9.4 RESET\_n Circuit Wiring

QRESET\_n will be wired as a long fly-by connection with the RCD at one end for each SDRAM channel. Connection will be from the RESET\_n pin of the RCD to the RESET\_n pin of each SDRAM in a daisy chain manner for each channel. Figure 15 demonstrates one possible wiring for this circuit.

The RESET\_n input pin of the RCD is connected to the RESET\_n pin of the edge pin connector. RDIMMs with PMIC5030 daisy-chain the system reset signal from edge pin to RCD and then to PMIC5030.



**Figure 15 — Example Wiring of the RESET\_n, QRESET\_n**

## 6.10 ZQ Calibration Wiring

DDR5 SDRAMs have a ZQ pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All DIMMs must connect a  $240\ \Omega \pm 1\%$  resistor from this pin of each SDRAM to ground (VSS).

The DDR5RCD0x register has a ZQCAL pin. This is intended to calibrate the on-die resistors for the drivers and the terminations. All DIMMs must connect a  $240\ \Omega \pm 1\%$  resistor from this pin of the register to ground (VSS).

All components that have a ZQ pin must have their own ZQ resistor. Sharing is not allowed.

## 6.11 Sideband Bus Signal Wiring, Selection, and Placement

This group contains Host SCL, SDA and SA signals, and Local SCL and SDA signals. The Host signals wire from the edge connector pin to SPD Hub pin. The Local signals fan out from the SPD Hub pin to PMIC, RCD, Temperature Sensor 0 and Temperature Sensor 1 in a star topology.

Even though these are considered slow speed signals in I2C or I3C-Basic mode operation it is paramount that routing is such to minimize signal integrity impact. Signals should be kept away or shielded from noisy signals. Refer to the individual content of each RDIMM Annex and Raw Card for how implemented.

The power supply rails for the SB are supplied from the PMIC and wire to the SPD Hub, RCD, and both temperature sensors in a star topology. Keeping these from noisy signals is crucial for the SB to properly operate.

The DIMM vendor is responsible for ensuring that the SB topology is optimized for operation.

6.11 Sideband Bus Signal Wiring, Selection, and Placement (cont'd)

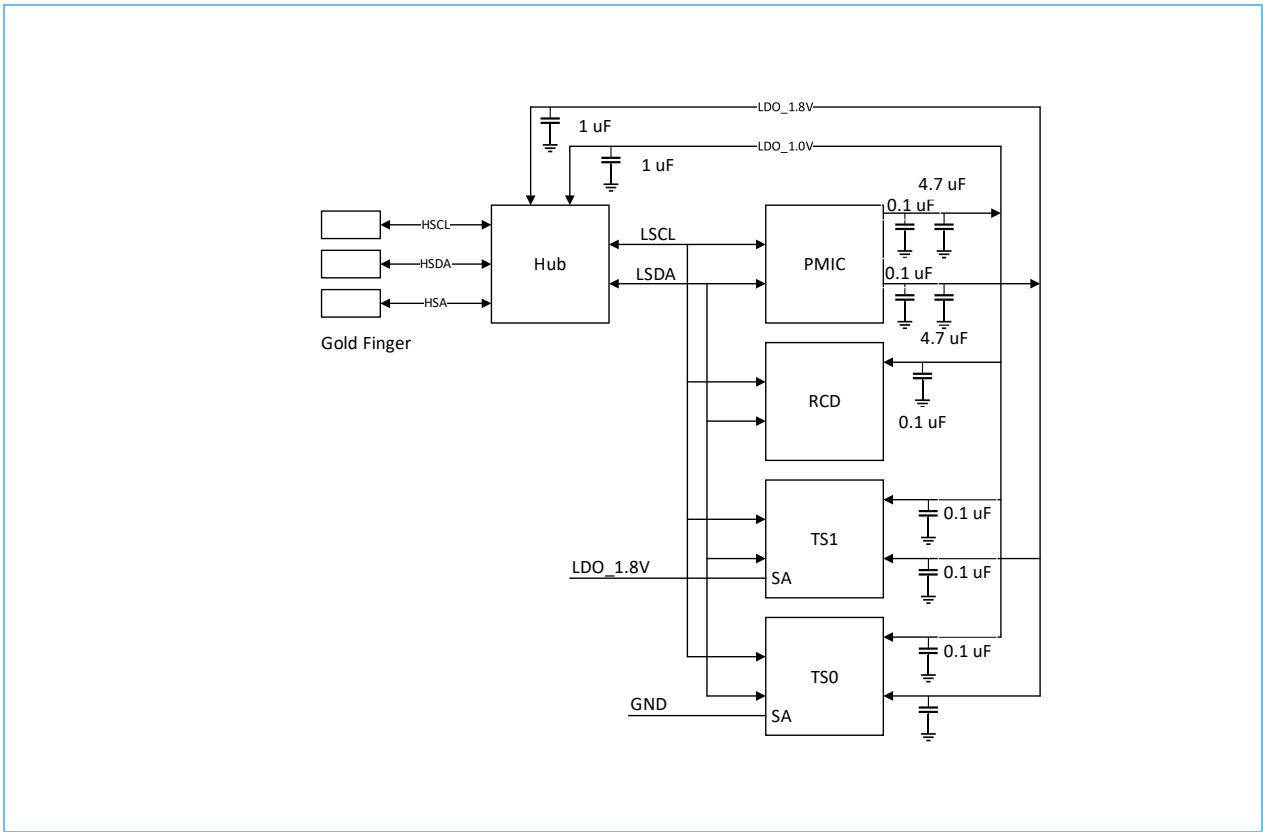


Figure 16 — Sideband Signal and Power Topology Example

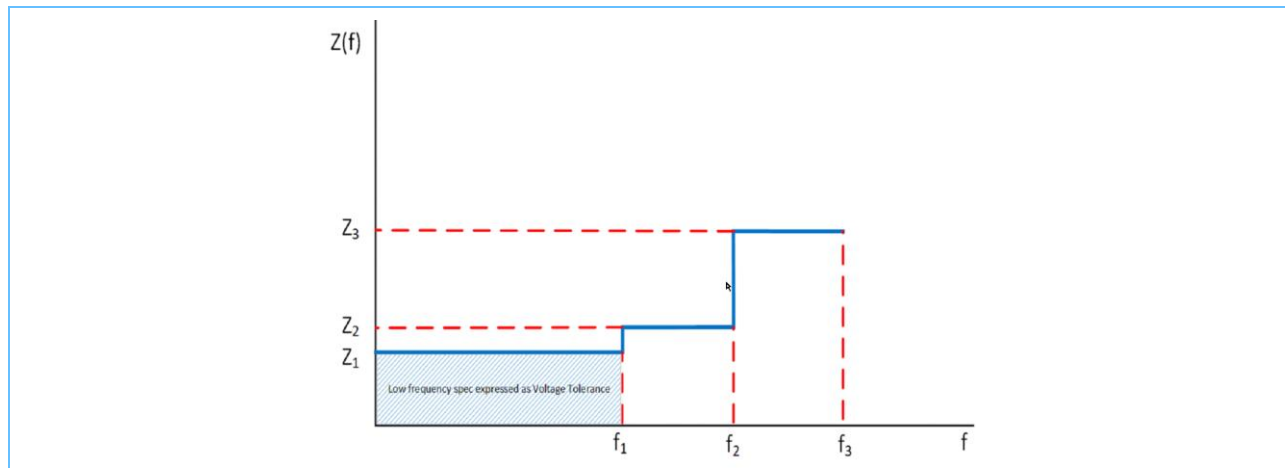
Table 18 — SMBus Lengths

SMBus Signals	Gold Finger to Hub	<= 108 mm		
	Hub to PMIC	<= 10 mm		
	Hub to RCD	<= 25 mm		
	Hub to TS00 (Ch-B)	<= 85 mm	If possible, match these lengths to within a few mm.	
	Hub to TS01 (Ch-A)	<= 85 mm		
NOTE 1 DIMM suppliers may adjust each length.				
NOTE 2 Via travel in not included in length.				

## 7 DIMM Impedance Profile

Applies to VDD, VDDQ, and VPP voltage rails. Profile may differ for different SDRAM devices (x4, x8, and 3DS).

Frequency ranges  $f_1$ ,  $f_2$ , and  $f_3$  are defined as:  $f_1 \leq 2$  MHz;  $f_2 = 10$  MHz;  $f_3 = 20$  MHz



$Z(f)$  targets for each frequency range ( $Z_1$ ,  $Z_2$ ,  $Z_3$ ).

$Z_x$  is expressed as voltage tolerance based on SDRAM input supply tolerances (-3%, +6%)

**Figure 17 — Impedance Profile**

**Table 19 — Example of Voltage Operating Conditions (for SDRAM)**

SDRAM	Symbol	Voltage Specification Freq: DC to 2 MHz				Z(f) Specification Freq: 2 to 10 MHz		Z(f) Specification Freq: 10 to 20 MHz		Notes
		Minimum (-3%)	Typical	Maximum (+6%)	Unit	$Z_{\max}$	Unit	$Z_{\max}$	Unit	
Core Power	VPP	1.746	1.8	1.908	V	100	mOhm	170	mOhm	3,4,5
Supply voltage	VDDQ	1.067	1.1	1.166	V	40	mOhm	80	mOhm	1,2,3,4,5
Supply Voltage	VDD	1.067	1.1	1.166	V	30	mOhm	50	mOhm	1,2,3,4,5
NOTE 1 DIMM operation must maintain volage rails at the SDRAM locations within those defined by JEDEC Standard JESD79-5.										
NOTE 2 VDDQ must be less than or equal to VDD. VDD must be within 66 mV of VDDQ.										
NOTE 3 AC parameters are measured separately on VDD and VDDQ.										
NOTE 4 DC to 2 MHz voltage range includes all noise at SDRAM ball, both DC and AC ripple fluctuations.										
NOTE 5 Z(f) is per voltage domain per SDRAM device. Per SDRAM BGA pin is not required.										
NOTE 6 Z(f) does not include the SDRAM package and silicon die.										
NOTE 7 DIMM vendors to verify the impedance with models reflecting the BOM.										

The Annex Standard will contain specific conditions and impedance for each raw card.

## 8 Electrically Induced Physical Damage (EIPD) Protection

For RDIMM raw card designs which contain protection devices.

Protection is provided to the VIN\_BULK rail with a discrete fuse and a discrete transient voltage suppressor (TVS). Protection is provided to the VIN\_MGMT rail with a discrete transient voltage suppressor (TVS).

The Fuse will be a 0603 (1610 metric) footprint in artwork. Fuse will be a mechanical one-time 7A datasheet rated element. DIMM suppliers will select suppliers and part numbers for their BOM. The fuse will be placed close to the edge connector pins and before any other device on the VIN\_BULK rail e.g., TVS and capacitor. The adjacent layer flooding under the VIN\_BULK edge pin supply copper shapes and supply side fuse pad will be voided of copper.

The VIN\_BULK TVS will be a 0603 (1610 metric) footprint in artwork. The DIMM supplier may substitute with a 0402 (1006 metric) footprint provided protection is similar. The TVS will be placed immediately after the fuse in artwork. If unable to place near the Fuse, then the TVS will be placed near the PMIC. The TVS is to be unidirectional with VRWM rated at a minimum of 15 V and typical of 16 V. Vclamp rating to be less than or equal to the PMIC Electrical Overstress voltage standard indicated. Other electric features of the TVS to be selected by the DIMM supplier. The DIMM supplier will select the TVS supplier and part number to be used in their BOM.

The VIN\_MGMT TVS will be an 0402 (1006 metric) footprint in artwork. The TVS for this raw card will be placed near the VIN\_MGMT edge connector pin if space allows, and before any other component on the rail e.g., capacitor. If unable to place near the edge connector pin, then the TVS will be placed near the PMIC. If unable to place near the edge connector pin, then the TVS will be placed near the PMIC. See the Annex for raw card placement location. The TVS can be unidirectional or be bi-directional with VRWM rated at a minimum of 3.6 V and typical of 4 V. Vclamp rating to be less than or equal to the PMIC Electrical Overstress voltage standard indicated. Other electric features of the TVS to be selected by the DIMM supplier. The DIMM supplier will select the TVS supplier and part number to be used in their BOM.

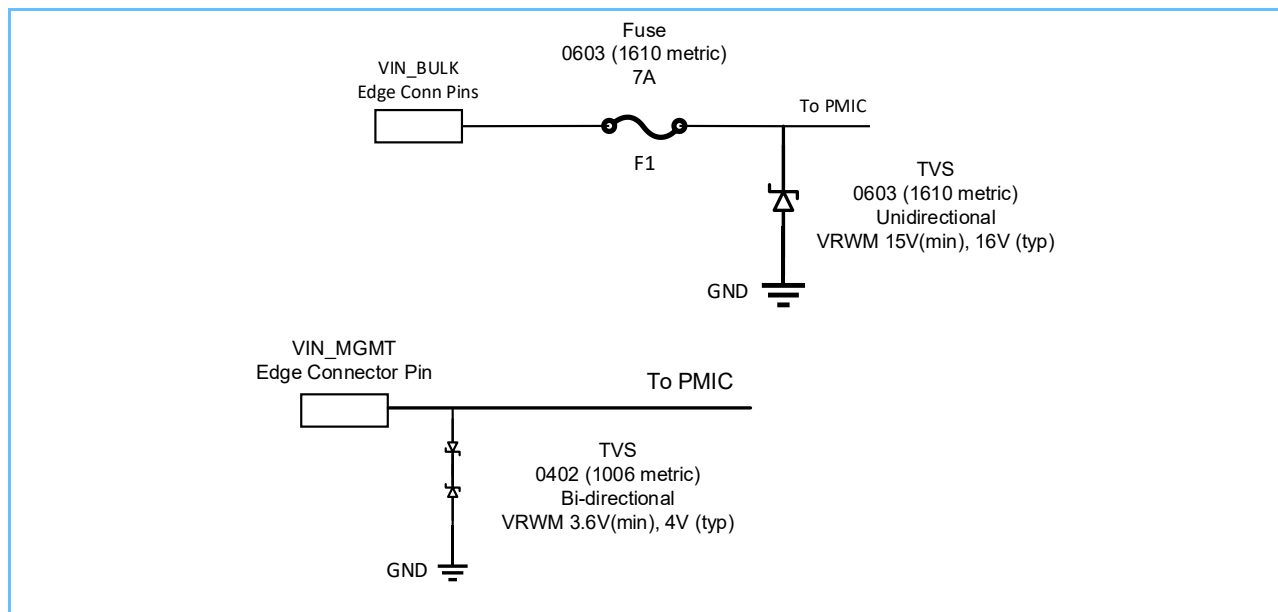


Figure 18 — Voltage Rail Protection

## 9 Reference Stackup

See Annex for reference design stackup.

**Table 20 — Example (10-layer) RDIMM Stackup**

Layer	Signal Description	Single-Ended Impedance		Copper (oz)	Dielectric Thickness (μm)
		Trace Width (μm)	Impedance (Ω)		
1	Addr / Ctrl	93	50	3/8 + Plating	
	DQ	190	35		
	Clock	270	25		
	Misc	93	50		
	Dielectric				75
2	Plane			1/2	
	Dielectric				70
3	Addr / Ctrl	74	50	1/2	
	DQ	145	35		
	Clock	248	25		
	Dielectric				115
4	Plane			1/2	
	Dielectric				70
5	Addr / Ctrl	63	50	1/2	
	DQ	136	35		
	Dielectric				115
6	Plane / Misc	63	50	1/2	
	Dielectric				122
7	Plane			1/2	
	Dielectric				115
8	Addr / Ctrl	74	50	1/2	
	DQ	145	35		
	Clock	248	25		
	Dielectric				70
9	Plane			1/2	
	Dielectric				115
10	Addr / Ctrl	93	50	3/8 + Plating	
	DQ	190	35		
	Misc	93	50		

## **10 Manufactured DIMMs**

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The Annex Standard documents a reference design that is intended to provide a solution that meets a set of specific requirements. There will always be improvements that can be made.

To allow manufactured DIMMs to be improved over the reference design, or to accommodate other SDRAM packages, minor changes to the trace lengths as defined in the length tables of a specific annex is allowed as long as the signal group skew is equal to or reduced relative to the reference design. It is a requirement that improvements are not made that move the basic timing away from the reference design such that system integrity is jeopardized for systems defined to operate with the original reference design. To restrict the degree of change so that basic timing is maintained, the identified net for each table must meet the trace lengths defined for that table.

To improve reference design, the manufacturer must establish a baseline for the reference design. Any improvements to the baseline must have reduced skew relative to the baseline. The baseline may have different skew values compared to the Annex. The simulation environment and tools are the likely source of differences between the baseline and the Annex. Significant differences should be brought to the attention of the reference design sponsor or JEDEC in general.

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## **11 Serial Presence Detect Definition and Content**

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This section is included for convenience. Refer to the DDR5 SPD Contents Standard (e.g., JESD400-5) for specific Addressing and Block information. Annex will contain SPD byte information specific to the raw card.

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## **12 Product Label**

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Please refer to JESD401-5 for the most up to date label standard.

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## **13 JEDEC Process**

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JEDEC provides PCB reference designs for DIMMs. The designs are divided into families. Registered DIMM is one of those. Letters (A, B, C, etc.) are used to define specific configurations (raw cards) of DIMM such as 2 rank with x4 based SDRAMs. Additional characteristics may further refine cards into specific raw card (RC- or R/C-) letters. Letter assignments are arbitrary and usually chronological. There is no other association to the letter assignments.

Raw Cards are reviewed and balloted by JEDEC members of TG451\_1 before being placed on the JEDEC website as a reference design. This is called a “Registration”. The initial registration is 0. A specific raw card may be the registration of R/C A0 as example. Subsequent design updates to the reference design go through the same balloting process and increment the registration number from 0 to 1 or the next highest number.



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## **Annex A — (Informative) Differences between Document Revisions**

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### **A.1 Differences between JESD305A\_2.00 and JESD305\_v1.00 (January 2022)**

- Changed cover title to remove LRDIMM
- Additional LRDIMM references removed from document
- Updated Table of Contents, List of Tables, and List of Figures
- Section 6.6.1 – Split Pre-RCD and DQ/Strobe into two sections. “Change Rank DIMM” with “Load”
- Add EOS section
- Updated many figures all throughout the document
- Updated EOS Protection wording
- Updated compensation formulas
- Minor editorial (DRAM to SDRAM, delete LR references, typo, etc.)
- EOS changed to EIPD
- Reference for 6400 added
- Minor editorial edits (e.g., spell out JESD standards, PMIC's, etc.)
- Removing Impedance target section in Table 15 (Section 6.4 contains same info)
- Add MO-xxx for active devices
- Many figures recreated (in Visio). Topologies did not change.
- Section 6.6 for Length Rules updated to match latest consensus.
- Table 14 and 15 – Added Consensus rules.
- Add JESD301-1, JESD301-4, JESD300-5 to Table 1
- Add JESD301-4 to Table 8
- Update EIPD wording to allow TVS's to be placed near PMIC if unable to place near edge connector pin
- Added 24Gb to SDRAM Supported and Module capacity to Table 1
- Rules for allowed variation: sec 4 and 5: removed texts “Pre and”
- Corrected trace width: Outer 0.90 -> 0.07 Inner 0.60 -> 0.05 in Table 16

## A.2 Differences between JESD305B\_v3.00 and JESD305A\_v2.00 (August 2025)

- Editorial corrections:
  - Vin\_Bulk to VIN\_BULK and Vin\_Mgmt to VIN\_MGMT all throughout
  - “specification” to “standard”
  - “Nom” to “Nominal”
  - Updated all table and figure numbering, including cross references
- Add/update content throughout to align with raw cards 8000 to 9200 Mbps
- Major detours from prior raw cards are instantiation of PMIC5030, and use of QCK twin-clock topology.
- Section 1: “...PC5-7200 support.” to “...PC5-9200 data rate support.”
- Clauses 1.1, 4.2, and 4.3: Added JESD301-5 - PMIC5030 Power Management IC Standard
- Tables 1 and 8: Added JESD301-5
- Table 5: Title update “Pin” to “Position”, changed Back side / Pin label to “RFU / No Pin Present” and added NOTE 2 for Pin 220 placement
- Table 6: Add 5030 to NOTE 5, corrected VPP max voltage typo from 1.098 to 1.908
- Section 5: Added JESD301-5 and updated the RCD and MO number (....JESD82-511/512/513/514 with MO-330, and JESD82-515 with MO-361).
- Clause 5.1, 2<sup>nd</sup> paragraph: Clarified component type and placement
- Table 8: Updated to “PMIC Standard” rather than each PMIC#
- Table 12: Added “Daisy Chain” to title
- Figure 6: New figure that describes “Y” topology used for 8000 Mbps and higher
- Clause 6.2.5: Changed heading title to “Post-RCD Control Signal Group”
- Clause 6.2.6: New clause for “Post-RCD Clock Signal Group”
- Figure 8: New figure for “Post-RCD QCSK Daisy-Chain Topology for Raw Cards through 7200 Mbps”
- Figure 9: Modified to “Post-RCD QCK Twin-Clock Topology for 8000 to 9200 Mbps Raw Cards”
- Table 14: Modified for QCA 1Rx8 Frontside SDRAM and added VR\_OE MIR
- Table 15: Updated consensus signal group length rules
- Table 17: Modified the reference design targets; LCSL, LSDA – Note superscript removed; Added ZQ = 50 ohm; Added LB Note #2
- Clause 6.2.7: “to be” removed from last paragraph
- Clause 6.4: Modified the reference design targets
- Clause 6.6.1: Added “TL2/1.1” to “Two SDRAM Loads” compensation
- Clause 6.6.4: Updated length match rules; definition of QCS\_n and less than 8000 Mbps QCK\_t/c; QCK\_t/c for 8000 Mbps and higher
- Clause 6.9.1 Figure 12: Modified wiring for 1Rx8 <8000 Mbps and  $\geq$  8000 Mbps
- Figure 15: Modified to add Reset\_n wiring for Gen 2 RDIMMs with PMIC5030
- Figure 16: Changed “Host” to “Gold Finger”; updated TS0 (GND) and TS1 (1.8V)
- Table 18: Updated SMBus Signal Lengths
- Table 19: Added NOTE 1



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**Standard Improvement Form****JEDEC JESD305B**

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

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3103 10th Street North  
Suite 240S  
Arlington, VA 22201

E-mail: [angies@jedec.org](mailto:angies@jedec.org)

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**1. I recommend changes to the following:**

☐ Requirement, clause \_\_\_\_\_

☐ Test method \_\_\_\_\_ Clause \_\_\_\_\_

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other \_\_\_\_\_

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**2. Recommendations for correction:**

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**3. Other suggestions for document improvement:**

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**Submitted by**

Name: \_\_\_\_\_

Phone: \_\_\_\_\_

Company: \_\_\_\_\_

E-mail: \_\_\_\_\_

Address: \_\_\_\_\_

City/State/Zip: \_\_\_\_\_

Date: \_\_\_\_\_

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